Generiek technologieplatform voor het integreren
van micro-elektronica en microfluïdica op rekbare substraten

Generic Technology Platform for the Integration
of Microelectronics and Microfluidics on Stretchable Substrates

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Gent, 28 februari 2013
Rik Verplancke

Table of Contents

List of Figures

List of Tables

List of Acronyms

A

ACA	Anisotropic conductive adhesive
ADC	Analog-to-digital converter
APTES	3-aminopropyltriethoxysilane
APTMS	3-aminopropyltrimethoxysilane

B

BAL	Bioartificial liver
BCB	Benzocyclobutene

C

CMOS	Complementary metal oxide semiconductor
CMP	Chemical mechanical polishing
CMST	Centre for microsystems technology
CTE	Coefficient of thermal expansion

D

DAC	Digital-to-analog converter
DBG	Dicing before grinding
DBS	Deep brain stimulation
DbyT	Dicing by thinning
DI	Deionized water
DOE	Design of experiments
DRIE	Deep reactive ion etch

E

ECG	Electrocardiogram
ENIG	Electroless nickel immersion gold

F

FEA	Finite element analysis

I

IC	Integrated circuit
ICA	Isotropic conductive adhesive
IPA	Isopropyl alcohol
ITRS	International technology road map for semiconductors
IWT	Agency for innovation by science and technology

L

LED	Light-emitting diode

M

μCP	Microcontact printing
μFSRFEs	Microfluidic stretchable radio frequency electronics
μTM	Microtransfer molding
MEA	Microelectrode array
MIMIC	Micromolding in capillaries
MSDS	Material safety data sheet

N

NMP	n-methyl-2-pyrrolidone

P

PCB	Printed circuit board
PD	Photodiode
PDMS	Polydimethylsiloxane
PET	Polyethylene terephthalate
PI	Polyimide
PMMA	Poly(methyl methacrylate)
PTCE	Packaging test chip version E

R

REM	Replica molding
RIE	Reactive ion etching
RISC	Reduced instruction set
rpm	Revolutions per minute
RT	Room temperature

S

sccm	Standard cubic centimeters per minute
SEM	Scanning electron microscope
SMD	Surface mount device
SMU	Source measure unit
SMEA	Stretchable microelectrode array
SOI	Silicon on insulator
SU-8	Negative tone, epoxy based photoresist from MicroChem

T

TFT	Thin-film transistor
TSV	Through-silicon via

U

USA	Ultrasonic agitation

UTCP	Ultrathin chip package
UV	Ultra violet

V

VCSEL	Vertical-cavity surface-emitting laserdiode

W

WYKO	Non-contact optical profilometer from Veeco

Z

ZIF	Zero insertion force

Samenvatting

In traditionele elektronische systemen worden de elektronische componenten op een substraat gemonteerd, en elektrisch verbonden met behulp van geleiders. Veelal wordt er gebruik gemaakt van rigide substraten, zoals printplaten (PCBs), maar er zijn ook flexibele varianten, zoals polyimide folies. Deze laatste categorie biedt aanzienlijk meer bewegingsvrijheid dan zijn rigide tegenhanger, hoewel de toegelaten mechanische vervormingen nog vrij beperkt blijven doordat de gebruikelijke elektronische materialen zoals metalen niet bestand zijn tegen de mechanische spanningen die met dergelijke vervormingen gepaard gaan. Bovendien wordt de flexibiliteit van het afgewerkte systeem vaak beperkt door de assemblage van dikke rigide elektronische componenten. In de huidige tendens waarbij steeds meer componenten op een kleiner oppervlak worden geplaatst, boet het afgewerkte systeem steeds meer aan flexibiliteit in.

Nochtans is er een toenemend aantal toepassingen waarbij flexibele elektronische schakelingen een grote meerwaarde kunnen bieden door nauw aan te sluiten en zich al dan niet dynamisch te kunnen aanpassen aan willekeurige vormen. Het aantal nieuwe toepassingen is omvangrijk en omvat biomedische systemen zoals rekbare matrices van micro-elektrodes, geavanceerde chirurgische instrumenten of draagbare monitorsystemen, bvb. elektrocardiogram (ECG) of temperatuursensoren. Deze systemen zijn in staat de gegevens van de patiënten te registreren, waarbij deze laatste niet noemenswaardig aan comfort hoeft in te boeten. Ook in andere toepassingsgebieden is er een vraag naar dergelijke elektronische schakelingen. Zo wordt er consumentenelektronica ontwikkeld die mechanisch kunnen vervormen (bvb. mobiele telefoons), daar waar de term 'curvilinear electronics' verwijst naar elektronische systemen die nauw aansluiten aan vloeiende driedimensionale vormen. Het maken van driedimensionaal vervormbare elektronische systemen vereist, naast flexibiliteit, ook dat het systeem in min of meerdere mate kan uitgerokken worden.

Zowel in de gezondheidssector als in de wereld van de microbiologie zijn er toepassingen te vinden voor rekbare elektronica, wanneer deze gecombineerd kan worden met microfluïdische systemen. Men zou bijvoorbeeld kunnen denken aan toestellen die het mogelijk maken om medicijnen of insuline toe te dienen, waarbij de dosis wordt aangepast na een *in situ* analyse van het bloed. Zo'n toestellen zijn bij voorkeur licht en compact, en kunnen zich in de mate van het mogelijke onopgemerkt aanpassen aan de vormen van de omgeving. Bij stamcel-

onderzoek is er dan weer een duidelijke nood aan zogenaamde multi-variabele platformen die het mogelijk maken om stamcellen simultaan mechanisch te rekken en elektrische metingen of stimulaties uit te voeren, terwijl de cellen zich in een nauwkeurig gecontroleerde fysiologisch relevante omgeving bevinden. Om aan de vereisten van dergelijke toestellen en onderzoeken te voldoen, werd in het kader van dit doctoraatsonderzoek een platform ontwikkeld gebaseerd op een generische technologie. Hierin spelen rekbare elektronica enerzijds en microfluïdica anderzijds een hoofdrol als basis bouwblokken. De ontwikkeling en de vervaardiging van deze bouwblokken vormt het onderwerp van de verscheidene hoofdstukken van dit proefschrift.

In de literatuur zijn vandaag verschillende strategieën terug te vinden om rekbare elektronica te realiseren, elk met zijn unieke voor- en nadelen. Twee conceptueel verschillende, doch complementaire strategieën kunnen aangewend worden. In de ene strategie wordt gebruik gemaakt van nieuwe elektronische materialen, zoals intrinsiek rekbare, geleidende composiet eleastomeren, in conventionele lay-outs. De andere strategie is daarentegen gebaseerd op het gebruik van conventionele hoogperformante (niet-rekbare) anorganische elektronische materialen in nieuwe structurele lay-outs. Ingenieuze structurele lay-outs zorgen ervoor dat een zekere rekbaarheid geïntroduceerd wordt. Hoofdstuk 1 geeft een grondig overzicht van de state of the art van rekbare elektronica.

In Hoofdstuk 2 wordt het gebruikte concept voor de realisatie van vervormbare, rekbare elektronica geïntroduceerd. Er wordt een versnipperde architectuur bevestigd op een elastisch substraat vooropgesteld: verscheidene niet-rekbare eilanden worden met elkaar verbonden met behulp van rekbare elektrische interconnecties, die toelaten het elastisch substraat te vervormen zonder de functionaliteit in het gedrang te brengen. Meanderende, hoefijzervormige metalen geleiders en het verdunnen van chips worden in detail beschreven; deze vormen immers de basis van de gebruikte strategie. Daarenboven wordt dieper ingegaan op een aantal microfabricatie technieken voor microfluïdische systemen: zowel traditionele technieken als technieken gebaseerd op 'soft-lithography' worden besproken om polydimethylsiloxaan (PDMS) van patronen te voorzien. Het hoofdstuk eindigt met een overzicht van de verschillende materialen die gebruikt worden voor de realisatie van een rekbare verpakking: de metalen geleiders, het type polyimide en de verscheidene siliconen worden besproken, en hun eigenschappen worden in detail bestudeerd.

In Hoofdstuk 3 wordt dieper ingegaan op de realisatie van rekbare elektrische interconnecties met behulp van meanderende, hoefijzervormige metalen geleiders, verpakt in een silicone elastomeer zoals PDMS. In deze configuratie gedragen de metalen geleiders zich als 'tweedimensionale veren'. Ten einde de mogelijkheid tot biomedische toepassingen te behouden werd ervoor gekozen om gebruik te maken van goud metallisatie, aangebracht met dunne-film technieken. De geleiders worden ondersteund door een polyimidelaag die de meanderende structuur volgt. Deze laag ondersteunt niet alleen de metallische verbinding, maar

verbetert tegelijk de levensduur van de interconnecties wanneer deze cyclisch gerekt worden. Deze stelling wordt onderbouwd door teststructuren, bestaande uit hoefijzervormige interconnecties, ontworpen langs evenwijdige rechte lijnen tussen testcontacten, uitvoerig mechanisch te testen. Hiervan wordt op het einde van Hoofdstuk 3 een samenvatting gegeven.

De rekbare elektrische interconnecties vormen een cruciaal onderdeel van het eerder beschreven platform voor vervormbare, rekbare elektronica waarin gebruik gemaakt wordt van verdunde chips, zoals beschreven in Hoofdstuk 4. De architectuur heeft een versnipperd karakter zoals beschreven in Hoofdstuk 2: actieve elektronische componenten worden op structurele eilanden van een niet-rekbaar materiaal geplaatst, die op hun beurt verbonden zijn met behulp van de rekbare elektrische interconnecties zoals beschreven in Hoofdstuk 3. In tegenstelling tot de in literatuur gangbare aanpak om elektronische componenten via enerzijds conventionele verbindingstechnieken, of anderzijds met behulp van gespecialiseerde microfabricatie technieken op niet-rekbare eilanden te bevestigen, wordt in dit werk de nadruk gelegd op het inbedden van elektronische componenten in een dunne polyimide verpakking, onder de vorm van verdunde chips. De achterliggende gedachte van deze aanpak is gebaseerd op het feit dat silicium chips, of eigenlijk om het even welk materiaal, buigzaam worden wanneer ze voldoende dun zijn. Dit kan makkelijk verklaard worden door op te merken dat de grootte van de lokale mechanische spanningen in de chip sterk afneemt naarmate de dikte van de chip afneemt, en dit bij eenzelfde buigradius. Daarom worden chips verdund tot diktes van 20 µm - 30 µm, en ingebed in een dunne polyimide verpakking (~50 µm). De metallisatie die de communicatie met de chip verzorgt wordt uitgewaaierd in de vorm van meanderende, hoefijzervormige metalen geleiders bedekt met hetzelfde polyimide. Door deze tot slot te encapsuleren in een elastomeer, in dit geval silicone of PDMS, wordt een systeem verkregen dat kan rekken en buigen, dit laatste zelfs ter hoogte van de niet-rekbare eilanden. Het proces wordt gedemonstreerd door het verdunnen en verpakken van silicium chips waarop zogenaamde 'daisy chain' teststructuren gevormd kunnen worden. De yield van het vervaardigingsproces wordt gekarakteriseerd door middel van elektrische geleidbaarheidsmetingen.

Hoewel een verscheidenheid aan polymeren wordt gebruikt voor de realisatie van microfluïdische systemen, heeft PDMS een bijzonder status in dit onderzoeksgebied verworven, onder meer dankzij zijn lage kost en groot gebruiksgemak. Reliëfstructuren, aanwezig op SU-8 mallen, worden gekopieerd naar PDMS membranen via technieken gebaseerd op 'soft-lithography'. Deze technieken versnellen het maken van prototypes, doch vereisen geen cleanroom faciliteiten en maken handig gebruik van de flexibiliteit van PDMS. Hoofdstuk 5 behandelt PDMS-gebaseerde systemen voor microfluïdica, bestaande uit één of meerdere fluïdische lagen. Daartoe wordt er een methodologie beschreven voor het aligneren en verlijmen van meerdere lagen PDMS, die in een vroegere fase voorzien worden van microstructuren. Deze technieken worden vervolgens op-

nieuw gebruikt voor de integratie van membranen tussen meerdere fluïdische lagen. Er wordt tevens een methodologie voorgesteld om elektronica (bvb. sensoren) aan PDMS-gebaseerde microfluïdische systemen toe te voegen. Hiervoor wordt in het bijzonder gebruik gemaakt van de geïntegreerde-chip technologie die in Hoofdstuk 4 wordt voorgesteld.
In de eerste hoofdstukken worden verschillende technologieën beschreven voor de realisatie van vervormbare, rekbare elektronica en PDMS-gebaseerde microfluïdische systemen. In Hoofdstuk 6 worden een aantal nieuwe toepassingen voorgesteld die voordeel halen uit deze technologieën. Zowel elastische microsystemen met modulaire functionaliteiten als PDMS-gebaseerde microfluïdische systemen voor het kweken van celculturen worden besproken. Eerstgenoemde is gebaseerd op de ontwikkelingen en eerste resultaten behaald in het kader van 'BrainSTAR'. In dit IWT-SBO gefinancierd project worden draadloze microsystemen ontwikkeld om enerzijds hersencellen te stimuleren, en anderzijds hersenactiveit te registreren bij kleine diermodellen. Om de toepasbaarheid van de technologieën beschreven in Hoofdstuk 3 en Hoofdstuk 4 te illustreren, wordt een technologiedemonstrator ontworpen en vervaardigd rond de MSP430 microcontroller chips van Texas Instruments. De PDMS-gebaseerde microfluïdische systemen voor celcultivatie, anderzijds, zijn ontwikkeld in het kader van 'HEPSTEM', een IWT-SBO gefinancierd project dat tot doel heeft menselijke hepatocyten, stelaatcellen en sinusoïdale endotheelcellen te onwikkelen, vertrekkende van stamcellen. Er wordt een zogenaamde micro-lever bioreactor ontwikkeld, waarbij de *in vivo* cellulaire architectuur van de lever zo goed mogelijk wordt nagestreefd *in vitro*. In het bijzonder wordt er aandacht besteed aan de integratie van poreuze membranen in een microfluïdische omgeving.
Hoofdstuk 7 besluit dit proefschrift. De belangrijkste resultaten worden er samengevat, en er worden een aantal onderwerpen voor toekomstig onderzoek rond het thema van dit doctoraatswerk gesuggereerd.

Summary

Electronic circuits are traditionally composed of electronic components assembled on either rigid substrates, such as printed circuit boards (PCBs), or on flexible substrates, such as polyimide foils. Metallic conductors, present on the substrates, take care of the electrical connectivity. The latter class of substrates offers substantial improvements in freedom of motion over its rigid counterpart, although the deformations are still quite limited due to the inability of common electronic materials, such as metals, to cope with the corresponding deforming strains. Furthermore, the ability to bend is often reduced by the assembly of bulky rigid electronic components. The current trend towards increased component density on substrates makes the final assembly even less flexible.

Nevertheless, electronic circuits which can fully conform and dynamically adapt to arbitrary curved surface topologies are of interest in diverse areas of application. The range of emerging applications is vast and include biomedical systems such as stretchable microelectrode arrays, advanced surgical tools or wearable unobtrusive health monitors, e.g. electrocardiogram (ECG) or temperature sensors, which are capable of conveniently monitoring patients without compromising the comfort of the user. Applications can be found in other fields as well: consumer electronics, such as mobile phones, are envisioned to transform their mechanical configuration, while curvilinear electronics require electronic circuits to be conformably integrated with curved three-dimensional shapes. Aside from flexibility, a certain degree of stretching is required for the three-dimensional shaping of electronic systems.

The possibility to combine stretchable electronics with microfluidics can improve applications in health care or boost research in the field of microbiology. On the one hand, one could imagine devices that regulate drug or insulin delivery after *in situ* analysis of the blood. Such devices would desirably be unobtrusive, conformable, compact and lightweight. Within the field of stem cell research, on the other hand, there is an obvious need for so-called multi-variable platforms which allow for the simultaneous application of mechanical strains and electrical recording / stimulation, while allowing the cells to reside in a well-controlled physiologically relevant environment. In order to comply with the requirements of such devices and multi-variable platforms, a generic technology platform was developed within the frame of this doctoral research. Stretchable electronics and microfluidics were considered to be the main building blocks. The development

and the fabrication of these building blocks are the subject of the diverse chapters of this dissertation.

To date, a variety of strategies towards the realization of stretchable electronic systems have been reported, each characterized by their unique pros and cons. Stretchable electronics can be achieved in two conceptually different, but complementary approaches: one relies on the use of new materials in conventional layouts, whereas the other relies on conventional materials in new structural layouts. The former focuses on the development and use of new electronic materials such as intrinsically stretchable composite elastomer conductors; the latter involves the use of conventional high-performance inorganic electronic materials by devising ingenious structural designs to introduce stretchability. Chapter 1 provides a thorough overview of the state-of-the-art of stretchable electronics.

In Chapter 2, the concept for realizing conformable, stretchable electronics is introduced. A pixelated architecture fixated on an elastomeric substrate is proposed: various non-stretchable islands are connected by stretchable electrical interconnections, which are able to deform with the elastomeric substrate without compromising the functionality. Meandering horseshoe shaped metallic conductors and thinning of dies are described in detail as these technologies form the basis of the packaging strategy. In addition, microfluidic technologies are introduced: traditional and soft-lithographic techniques to pattern polydimethylsiloxane (PDMS) are reviewed. The chapter concludes with an engineering review on the materials which are used for the realization of a stretchable package. Several of the materials such as the metallic conductors, the type of polyimide and the diverse silicone elastomers are presented and their properties are discussed in detail.

Chapter 3 deals with the realization of stretchable electrical interconnections by encapsulating meandering horseshoe shaped metallic conductors in a silicone elastomer, i.e. PDMS. In this configuration, the metallic conductors are able to function as 'two-dimensional springs'. Thin-film gold metallization is applied via thin-film techniques and is used to retain the possibility of biomedical applications. Structured polyimide is introduced around the meandering conductors, and follows the meandering configuration: it serves as a support for the conductors and as such successfully improves the lifetime of the interconnections when cyclically subjected to strains. This hypothesis was demonstrated by fabricating test structures consisting of horseshoe shaped interconnections designed along straight parallel lines in between test pads. The test structures were mechanically tested; Chapter 3 ends by summarizing the results of these mechanical tests.

The stretchable electrical interconnections are a key aspect for the conformable, stretchable electronics platform using thin dies, presented in Chapter 4. It is based on the pixelated architecture described in Chapter 2: islands of a structural, non-stretchable material host active electronic components or subcircuits and are connected through the stretchable electrical wiring presented in Chapter 3. Whereas in related approaches electronic components are assembled on the

non-stretchable islands in conventional ways or require custom microfabrication, in this work focus is put on the implementation of electronic components by embedding them as thin dies in a slim polyimide package. The idea underlying this approach is that flexibility is improved as silicon dies, or any material for that matter, become flexible if sufficiently thinned. This is easily explained by noting that, for a certain bending radius, the magnitude of the bending strains in the die is greatly reduced as the thickness decreases. For this reason, dies were thinned to thicknesses of 20 µm - 30 µm and were embedded in a slim polyimide package (~50 µm), while the fan-out metallization is configured as polyimide covered meandering horseshoe shaped metallic conductors. By subsequent encapsulation in a silicone elastomer, i.e. PDMS, a system is achieved that can stretch and flex, the latter even at the location of the non-stretchable islands. The process is demonstrated by thinning and embedding so-called daisy chain silicon dies. The process yield is characterized via electrical conductivity measurements performed on the embedded dies.

Although various polymers have become popular in the field of microfluidics, PDMS in particular is of interest as it really has boosted research in the field of microfluidics due to its low cost and ease of use. Soft-lithographic techniques are used to replicate the relief structures present on the surface of a master mold fabricated via SU-8 photolithography. These techniques allow for rapid prototyping, do not require cleanroom facilities and benefit greatly from the flexibility of PDMS. Chapter 5 handles PDMS-based microfluidics consisting of single or multiple fluidic layers. To this end, an aligning and bonding methodology for multiple micro-patterned PDMS layers is described, and used for the integration of membranes in between multiple fluidic layers. Furthermore, a methodology is presented to add electronics (e.g. sensors) to the microfluidic devices. Particular attention is spent to combine the PDMS-based microfluidics with the technology presented in Chapter 4.

Whereas in previous chapters, technologies are presented for the realization of conformable, stretchable electronics and PDMS-based microfluidics, in Chapter 6 enabling applications are highlighted which benefit greatly from these technologies. Both elastic microsystems with modular functionalities and PDMS-based microfluidics for cell culturing are discussed. For the former, the focus is put on the developments and the initial results achieved within the frame of the IWT-SBO funded project 'BrainSTAR', which aims to develop wireless microsystems for brain stimulation and recording in small animal models. To illustrate the applicability of the technologies presented in Chapter 3 and Chapter 4, a technology demonstrator was designed and fabricated using the MSP430 microcontroller dies from Texas Instruments. Concerning the PDMS-based microfluidics for cell culturing, the focus is put on the developments and the initial results achieved within the frame of the IWT-SBO funded project 'HEPSTEM', which aims to develop functional human hepatocytes, stellate cells and sinusoidal endothelial cells from stem cells. A so-called micro-hepatic sinusoid bioreactor is

developed which has a cellular architecture closely resembling that of the liver *in vivo*. Specific attention is spent to the integration of porous membranes in a microfluidic environment.
Chapter 7 concludes this dissertation by summarizing the main achievements and recommending some interesting topics for future research.

1 Introduction

1.1 Conformable, stretchable electronics

Conventional electronic systems are composed of electronic components assembled on rigid substrates, such as printed circuit boards (PCBs), or flexible substrates, such as polyimide (PI) foils. The latter class offers substantial improvements in freedom of motion over its rigid counterpart, though deformations are still quite limited due to the inability of common electronic materials, such as silicon or metals, to cope with the corresponding deforming strains. Furthermore, the ability to bend is often reduced by the assembly of bulky rigid electronic components. The current trend towards increased component density on substrates makes the final assembly even less flexible. These two limitations clearly restrict the application space of electronics.

It is clear that maximizing the conformability requires a certain degree of flexibility, or even stretchability of the electronic systems. Recent efforts to increase the flexibility have been focusing mainly on the thinning of wafers and chips. This concept has already been reported as an enabler for applications requiring improved flexibility (e.g. retinal implants, RFID tags) [1, 2]. Furthermore, technologies, such as the ultra-thin chip packaging technology (UTCP), have been reported which exploit the thinning as a means to cope with the increased component density by embedding the components into the substrate [3, 4].

Introducing stretchability in electronic devices is a relatively new concept. Its origin can be traced back to a paper published in 2001, in which Lumelsky et al. survey the state-of-the-art and research issues that need to be resolved in order to

make sensitive skin a reality [5]. Sensitive skin was described as being a large array of sensors embedded in a flexible, stretchable and / or foldable substrate that might cover the surface of a moving machine or even a part of the human body. It was envisioned that sensitive skin devices will revolutionize important areas of the service industry by the use of unsupervised machines, make significant contributions to human prosthetics, and augment human sensing when fashioned into clothing. Since its publication, different research groups have significantly contributed to this new field of electronics called 'stretchable electronics'.

1.1.1 Distinguishing flexible and stretchable electronics

Flexible and stretchable electronics both render electronic systems mechanically deformable, enabling the integration of electronics (e.g. sensors and actuators) onto curved surfaces, inside restricted spaces, in contact with soft biological tissue, etc. However, flexibility is commonly attributed to developable surfaces, i.e. surfaces that can be flattened onto a plane without distortion (stretching / compression), whereas stretchability is typically considered a property of deformable surfaces, i.e. surfaces that conform to complex shapes once or many times or surfaces that can expand and relax reversibly [6].

Thin plastic or metal foils, which are common substrate materials for flexible systems, can conform to developable surfaces such as cylinders and cones, thereby coping with the corresponding small deforming strains. Consider e.g. a foil with thickness t, which is bent around a cylinder with radius ρ. The strain on its surface can be estimated as:

$$\epsilon = \frac{t}{2\rho + t} \tag{1.1}$$

Filling out the realistic numerical values t = 100 µm and ρ = 1 cm, the strain is estimated as ϵ = 0.5 %. Although this is an estimate, which can be made more accurate by including the different materials in the calculation, the conclusion remains true: the strains in flexible electronics can be made quite small, well below the fracture limits of the constituent materials.

Reversibly deforming flat substrates to non-developable, arbitrarily shaped surface topologies or dynamically adapting to moving surfaces is more demanding. In the process of deforming, the substrate is bent, twisted and / or uniaxially / multiaxially stretched. This requires the substrates to be stretchable, implying the use of less common substrate materials such as elastomers. Furthermore, also the electronic materials need to cope with the relatively large strains, exceeding the fracture limits of the constituent materials, without compromising the functionality of the system.

1.1.2 Applications

Stretchable electronics do not only provide the means to better integrate existing functionality, they are also considered an enabler of applications that are impossible to achieve with conventional rigid and flexible technologies. This new field has gained a lot of interest in diverse areas of application, such as health care, medicine and biomedical science. The ability to dynamically deform the mechanical form factor of a system to an arbitrary shape allows, for example, the monitoring of patients in their natural environments via e.g. electrocardiogram (ECG), electroencephalogram (EEG) or temperature sensors. Such wearable health monitors are capable of conveniently monitoring patients, and are preferably unobtrusive to avoid compromising the comfort of the user [7, 8]. Recently, also stretchable microelectrode arrays (Section 1.2.1) and advanced surgical tools, such as multifunctional inflatable balloon catheters, were suggested [9]. The latter contain e.g. tactile, temperature and flow sensors to provide critical information during surgery. In Section 1.2, the opportunities for cell culturing will be discussed in more detail.
Applications can, however, be found in other fields as well. Smart fabrics or intelligent textile benefit from stretchable electronics as it improves user comfort, and allows for a higher degree of integration of electronic devices in the fabrics [10, 11]. Consumer electronics such as mobile phones are envisioned to transform their mechanical configuration [12, 13]. Curvilinear electronics, on the other hand, require electronic circuits to be conformably integrated with curved three-dimensional shapes [14, 15]. Aside from flexibility, a certain degree of stretching is required for the three-dimensional shaping of electronic systems.

1.1.3 State-of-the-art

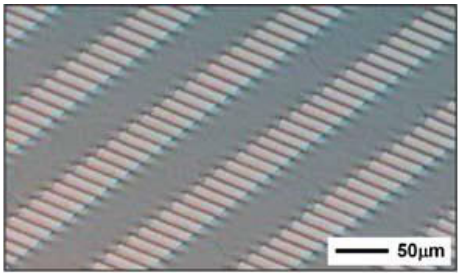
To date, a variety of strategies towards the realization of stretchable electronic systems have been reported. Stretchable electronics can be achieved in two conceptually different, but complementary approaches: one relies on the use of new materials in conventional layouts, whereas the other relies on conventional materials in new structural layouts. The former focuses on the development and use of new electronic materials such as intrinsically stretchable composite elastomer conductors; the latter involves the use of conventional high-performance inorganic electronic materials by devising ingenious structural designs to introduce stretchability. In this section, some selected approaches are outlined, each with their unique pros and cons.

Out of plane strategies

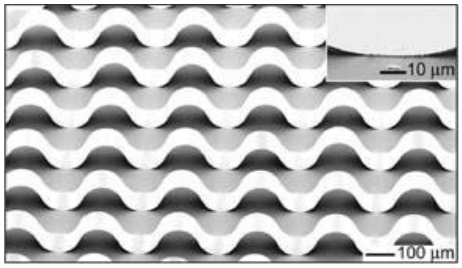
Strategies which are classified as 'out of plane' exploit out of plane motion in thin layers to accommodate strains applied in the plane. An elementary result in mechanics underlies this strategy: any material becomes flexible if sufficiently

thinned. This is easily explained by noting that the magnitude of the bending strains in the material is greatly reduced as the thickness decreases, while the bending radius is kept constant. By configuring such flexible materials in layouts that enable motion out of the plane of the circuit and bonding them to or embedding them in elastomeric substrates, stretchable systems are obtained. Both ultrathin semiconductor materials [14, 16–23] and very thin metal films [24–32] have been reported in this context.

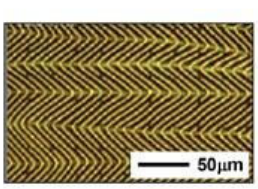
Ultrathin semiconductors Stretchable forms of ultrathin semiconductors such as silicon, gallium arsenide (GaAs), gallium nitride (GaN) or indium phosphide (InP) can be achieved by using wavy layouts, supported by an elastomeric substrate [14]. The fabrication starts with the generation of ultrathin structures of the semiconductors. These are transferred to an elastically (mechanically or thermally) prestrained PDMS elastomeric substrate through a technique called 'transfer printing' [16, 33, 34]. By releasing the prestrain, wavy configurations are obtained which can be reversibly stretched and compressed to large levels of strain without damage. The deformations are accommodated by changes in the wavelengths, amplitudes and spatial layouts of the wave structures, thereby avoiding destructive strains in the semiconductor itself.
The adhesion between the structures and PDMS is achieved by covalent -O-Si-O- linkages between silanol (Si-OH) groups on the PDMS surface, generated through a brief exposure to an oxygen plasma or ozone, and similar groups on layers of SiO_2 on the structures. Silicon structures can thus readily achieve adhesion through the native oxide; other structures such as gallium arsenide or polyimide are coated with a very thin layer of SiO_2 prior to the bonding.
Khang et al. applied this approach to nanoribbons of single-crystal silicon [17]. Silicon nanoribbons can be generated from high-quality bulk or layered wafers, e.g. through undercut etching of the buried oxide of silicon on insulator (SOI) wafers. The thickness of the top silicon on the SOI wafers, ranging from tens of nanometers to several hundreds of nanometers, defines the thickness of the nanoribbons. These are transferred to an elastically prestrained PDMS membrane by conformal contact between the substrate and the nanoribbons over their entire length. Mechanical relaxation yields wavy silicon nanoribbons, as illustrated in Figure 1.1(a), with amplitudes and wavelengths that are fixed and dependent primarily (but not exclusively) on the thickness of the nanoribbons and the moduli of the materials.
The uniformly bonded, wavy nanoribbons have two main disadvantages. First, they form spontaneously with little control over the geometry. Second, the maximum strains are limited by the non-optimal wave geometries, and are in the range of 20 % - 30 %. Therefore, Sun et al. reported an alternative approach which employs selective bonding of nanoribbons to an elastically prestrained PDMS substrate [18]. The selective bonding is achieved by selectively functionalizing the PDMS surface, e.g. by using a masking layer during its exposure to ozone.

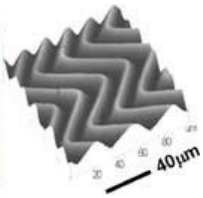


(a) Silicon nanoribbons in wavy configurations.

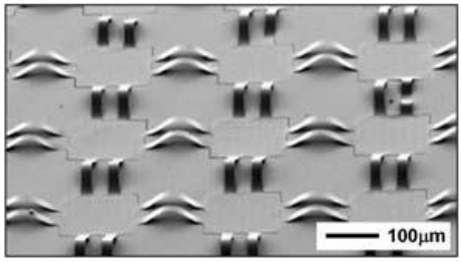


(b) Gallium arsenide nanoribbons in buckled configurations; bonding occurs only at the troughs.





(c) Wavy silicon nanomembrane.



(d) Buckled silicon nanomembrane; bonding is localized to the regions of the square islands.

Figure 1.1: Configurations of ultrathin semiconductor materials completely or selectively bonded to elastically prestrained PDMS substrates [14, 17–19].

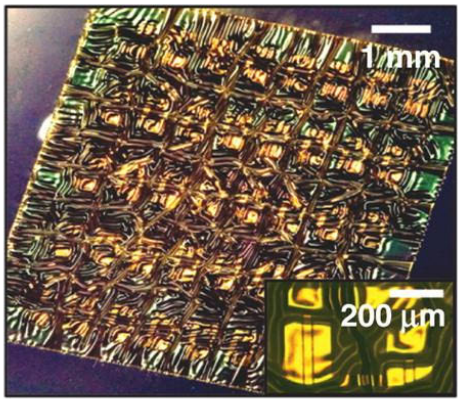
Release of the prestrain yields buckled configurations: non-bonded regions of the nanoribbons delaminate (or pop up) from the PDMS substrate, as illustrated in Figure 1.1(b). It is clear that this type of configuration offers close control over the buckling period, allowing optimization of the range of stretchability.

The same concepts can be applied to two-dimensional nanomembranes or mesh structures. Uniformly bonded silicon nanomembranes result in wavy shapes with herringbone layouts upon mechanical relaxation of the biaxially prestrained PDMS substrate, as displayed in Figure 1.1(c) [19]. The mesh structures in Figure 1.1(d) can be considered the two-dimensional analog of the selectively bonded, buckled nanoribbons: the square islands are bonded to the PDMS substrate, in contrast to the interconnections which pop up after releasing the prestrain [14]. Although the mechanics is more complex, the response to strain is similar: in plane strains are accommodated by changes in the wavelengths, amplitudes and spatial layouts of the wavy structures.

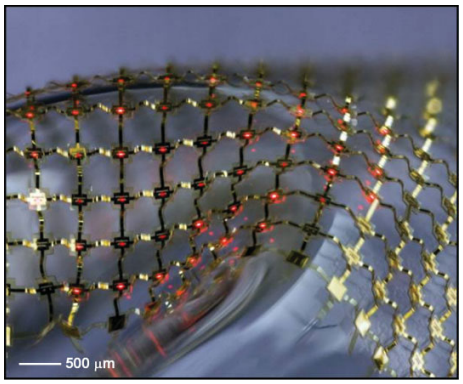
To demonstrate the capabilities of these techniques, several functional electronic

devices such as stretchable conductors, transistors, diodes, photodetectors and various circuits have been fabricated. Patterns of dopants, metallization and dielectric layers can be provided using conventional techniques prior to the fabrication process described above. Figure 1.2(a) displays a wavy silicon complementary metal oxide semiconductor (CMOS) circuit fabricated on a 1.2 µm thick polyimide film, prior to transferring it to a biaxially prestrained PDMS substrate [20]. It is noticed that circuits result in a more complex layout than those depicted in Figure 1.1, due to the heterogeneity of the circuits.
A disadvantage of the uniformly bonded wavy circuits is that the active devices are also subject to strain, possibly changing device performance. This can be minimized by using layouts which focus the strains to regions which are not or less sensitive to strain, such as the interconnections, e.g. by localizing the wavy structures or by using mesh layouts. The latter offers the extra advantage that the stretchability is increased. Figure 1.2(b) displays a representative device: a stretchable display consisting of 256 AlInGaP light-emitting diodes (LEDs), configured in a mesh layout with selectively bonded, buckled interconnections [21]. The straight arc-shaped bridges in the mesh layout can also be replaced with non-coplanar serpentine-shaped structures, as illustrated in Figure 1.2(c) [14]. These can provide an increased stretchability because they are able to accommodate larger prestrains due to their longer lengths, while the applied strain can also easily exceed the prestrain due to the buckling modes associated with the serpentine geometry. Furthermore, by fine-tuning the length, width and thickness of the serpentine shapes, stretchability can be further improved.

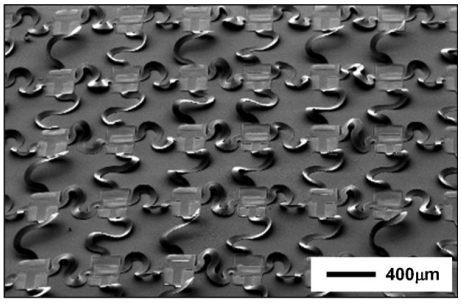
Very thin metal films Bowden et al. observed that periodic surface waves appear when thin metal films (typically 50 nm thick gold films with a 5 nm thick titanium or chromium adhesion layer) are deposited on a PDMS substrate by electron beam evaporation [35]. A group of researchers from Princeton University exploited this phenomenon to create stretchable metallization. They deposited very thin gold layers with thicknesses ranging from 20 nm to 100 nm, preceded by a 5 nm thick chromium adhesion enhancement layer, on a PDMS substrate by electron beam evaporation. Compressive stress, developed in the metal film during its deposition on the PDMS substrate, is released by random buckling or waves when the metal film extends over large surfaces, as shown in Figure 1.3(a). However, when the metallization is evaporated through a shadow mask to define conductor stripes, a pattern of parallel waves is developed, as shown for a 600 µm wide stripe in Figure 1.3(b).
While freestanding metal films have often been reported to fracture at strains of 1 % - 2 %, Lacour et al. reported that the wavy gold films can be stretched up to 22 %, and yet remain electrically conducting [24]. Moreover, stretchability can be further improved by prestretching the PDMS substrates prior to the deposition of the gold film. Similar morphologies are noticed, although cracks can appear along the length of the conductor due to tensile stress caused by the Poisson's

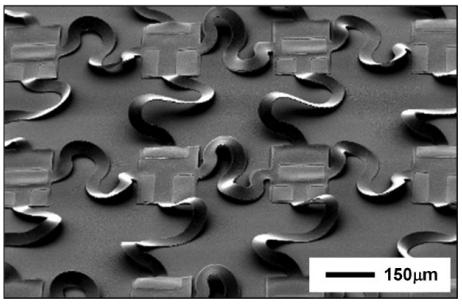


(a) Wavy silicon CMOS circuit.



(b) LED display in a straight arc-shaped mesh layout.





(c) Islands of transistors for CMOS inverters in a serpentine mesh layout.

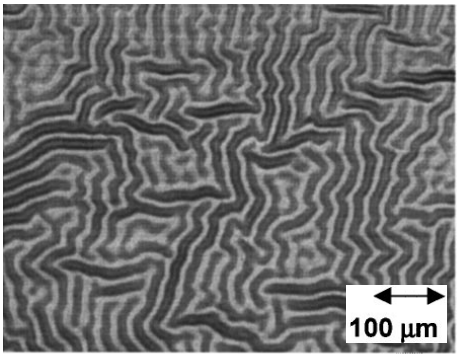
Figure 1.2: Functional stretchable electronic devices using ultrathin semiconductors [14, 20, 21].

effect; this is illustrated in Figure 1.3(c). Jones et al. reported that gold conductors deposited on PDMS substrates that are uniaxially prestretched by 25 %, can be stretched up to 100 % while remaining electrically conducting [25].
Aside from the two wavy topographies, also flat gold conductors deposited on relaxed PDMS substrates were reported to be stretchable [26–28]. The morphology of such a gold film is depicted in Figure 1.3(d): it contains a network of tri-branched microcracks with lengths of micrometers and less. When such gold films are deposited on a sufficiently compliant PDMS substrate, the microcrack pattern allows the metal film to accommodate strains in the plane: cracks open and close while metal ligaments deflect and twist out of the plane. Small, elastic strains are induced in the metal film, so that a finite and reproducible electrical resistance is maintained over repeated deformations [28].
To achieve stretchable electronic systems, rigid or flexible subcircuit islands composed of e.g. sensors, actuators and conditioning electronics are distributed over the PDMS substrate. The islands remain non-stretched and are connected by stretchable metallic conductors [29]. This concept was demonstrated with an inverter circuit composed of two amorphous silicon thin-film transistors (a-Si TFTs), fabricated on a 50 µm thick polyimide foil [26].

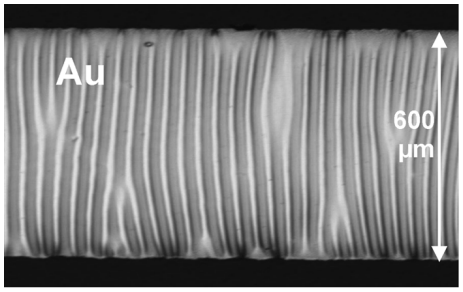
Coplanar strategies

Strategies which are classified as 'coplanar' do not use, or are not specifically designed to exploit, out of plane motion to accommodate strains applied in the plane. Quite diverse strategies have been reported ranging from metallic spring structures [36–40] to silicon spring structures [41–44] and microfluidic channels filled with liquid alloys [8, 45–50].

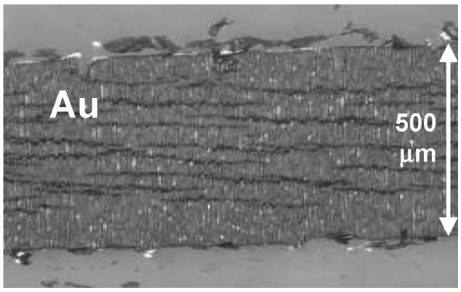
Metallic spring structures This strategy receives inspiration from Gray et al. [36]. The basic idea underlying this strategy is that many metals, which are unable to stretch significantly, are able to bend if their cross sections are sufficiently small. Therefore, in order to obtain stretchability, it was proposed to embed tortuous metallic conductors in an elastomeric substrate. The hypothesis was tested by using standard photolithographic techniques to embed both straight and tortuous gold conductors in PDMS. Figure 1.4 shows the conductors before, during and after uniaxially stretching in the direction indicated by the arrows. The dark regions indicate that out of plane buckling accompanies the bending to accommodate the applied strains. While electrical failure occurred at a strain of approximately 2.4 % for the straight conductors, the depicted tortuous conductors with low and high amplitude remained conductive up to strains of approximately 14.2 % and 27.2 %, respectively.
These results inspired other researchers, including the CMST research group, to develop alternative fabrication techniques, use other materials or to alter the design in order to improve stretchability and reliability of the interconnections.



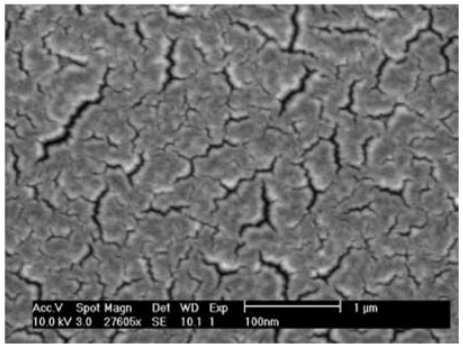
(a) Random waves in a gold film extending over a large surface.



(b) Parallel waves in a 600 µm wide gold conductor stripe.



(c) Waves formed after release of a 15 % prestretched PDMS substrate; cracks appear along the length of the conductor.



(d) Tri-branched microcracks in a flat film.

Figure 1.3: Surface topography of gold metallization evaporated on PDMS substrates [24, 26, 29].

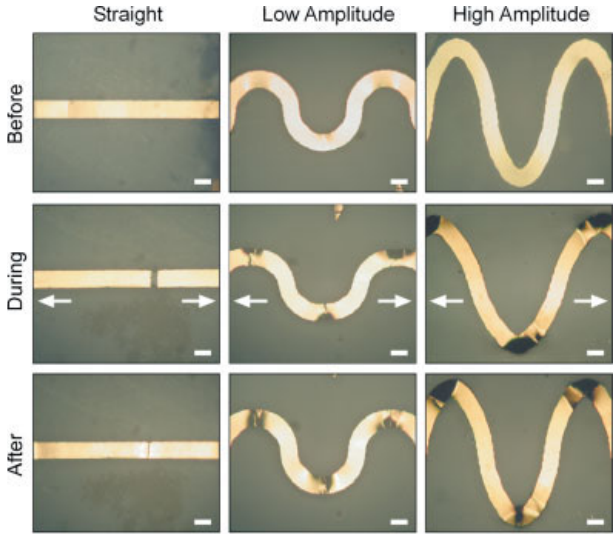
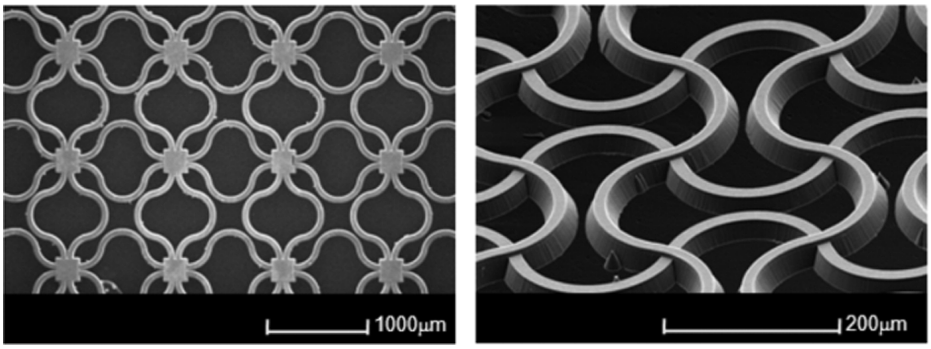


Figure 1.4: Gold conductors encapsulated in PDMS, before, during and after uniaxially stretching until the occurrence of electrical failure; scale bars are 100 µm [36].

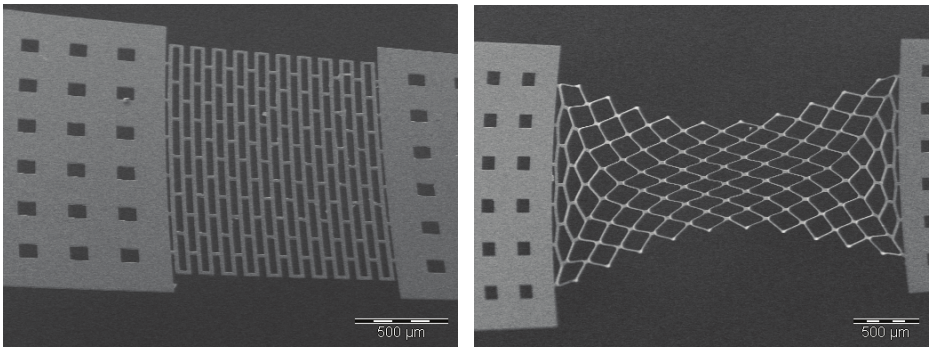
Since this strategy is of particular interest in this dissertation, it will be discussed in more detail in Chapter 2.
Related approaches do not use elastomeric substrates to support the metallic interconnections. Lin et al. developed stretchable interconnections based on excimer laser ablation of metalized polyimide sheets, which were then used in mesh-shaped designs with multiple levels of meandering metallization, as shown in Figure 1.5 [37, 38]. Sosin et al. fabricated and characterized the stretching of freestanding electroplated copper interconnections with meandering and mesh-shaped geometries, the latter of which is illustrated in Figure 1.6. [39]. This concept was then used in a CMOS compatible post-processing module to convert silicon electronics into large-area systems by plastic deformation of freestanding, mesh-shaped metallic interconnections [40].

Silicon spring structures As is the case with metals, also silicon can be shaped into two-dimensional spring structures. One such approach expands functional silicon dies by several orders of magnitude, by structuring the silicon die as a two-dimensional network of silicon islands and spring structures using a deep reactive ion etch (DRIE) process [41–43]. An example is shown in Figure 1.7(a): the springs are configured as 1.6 µm wide spiral ribbons that are wrapped around 200 µm diameter circular silicon islands; all structures have a thickness of 30 µm.



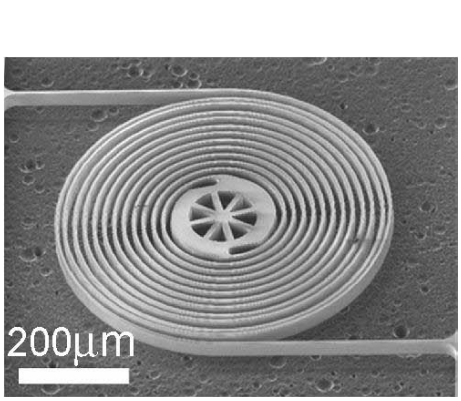
(a) Line-width: 40 µm. (b) Line-width: 20 µm.

Figure 1.5: Mesh-shaped designs with two levels of meandering metallization [38].

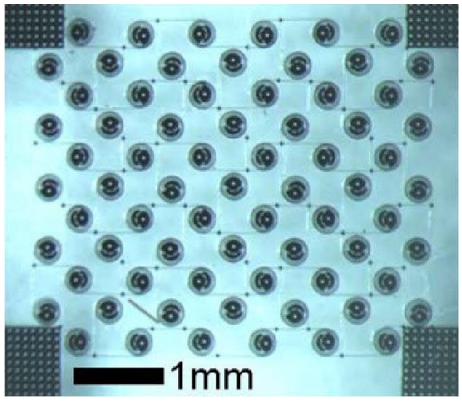


(a) Before stretching. (b) After stretching.

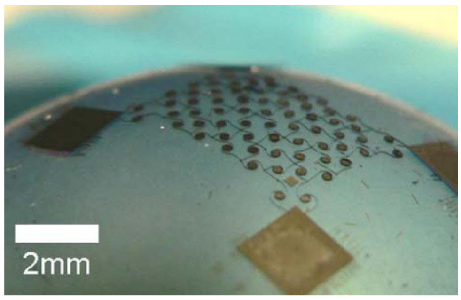
Figure 1.6: Freestanding mesh-shaped metallic interconnections [40].



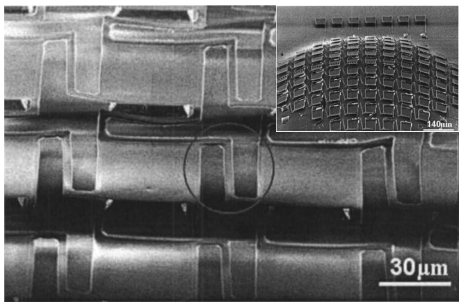
(a) Spiral ribbons wrapped around a circular island.



(b) Undeformed two-dimensional network.



(c) Two-dimensional network conformed to a curved surface.



(d) S-shaped microfabricated suspensions.

Figure 1.7: Silicon islands interconnected by spring structures [42, 44].

The islands can host active electronic devices (e.g. by structuring silicon wafers post-foundry) and are electrically connected to neighboring islands via one or multiple levels of metallization on the spiral ribbons. The organization into a two-dimensional network (Figure 1.7(b)) allows biaxial stretching and compression (Figure 1.7(c)). Strains are accommodated through a combination of unwinding of the spiral ribbons and rotation of the islands.

Hung et al. reported a similar strategy: silicon islands are interconnected by S-shaped microfabricated suspensions, as shown in Figure 1.7(d) [44]. The inset shows an array of interconnected islands on an inflated PDMS membrane.

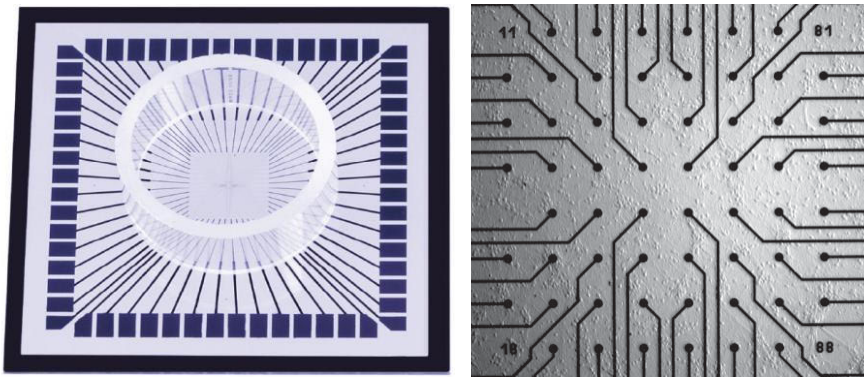
Microfluidic technologies This strategy takes advantage of the recent advances in PDMS-based microfluidic technologies. Siegel et al. reported a technique called 'microsolidics': molten solder is injected into networks of microfluidic channels in PDMS, fabricated using soft lithography, followed by cooling and solidification of the solder [45]. After fabrication, the metallic structures can be flexed, bent or twisted into a variety of shapes. Breaks or defects in the solder microstructures can be repaired by reflowing the solder.
To enable reversible stretchability, the solder can be replaced by room temperature liquid alloys. Kim et al. illustrated this concept using microfluidic channels in PDMS, having a typical height of 100 µm and widths ranging from 30 µm to 100 µm, filled with eutectic gallium indium alloy (EGaIn, gallium / indium = 75.5 / 24.5, melting point 15.7 °C) [46]. Electrical interconnections with a maximum stretchability of 100 % and limited resistance variations, caused by changes in the microfluidic channel dimensions when stretched, were achieved. The integration of active electronic devices was illustrated by inserting the legs of surface mount devices (SMDs) in liquid alloy filled reservoirs [46].
Follow-up papers report on the fabrication of several stretchable microfluidic antennas. Cheng et al. demonstrated the first stretchable antennas based on the eutectic alloy galinstan (gallium / indium / tin = 68.5 / 21.5 / 10), allowing stretching up to 40 % along any axis [47, 48]. Also antennas based on EGaIn were reported, including antennas which could be stretched up to 120 % [49, 50]. More recent work presented microfluidic stretchable radio frequency electronics (μFSRFEs) for which a hybrid integration strategy was used: all electronics (e.g. established ICs and discrete passive components) except the power supply were fully encapsulated in PDMS [8].

1.2 Microengineering for biological studies

Microengineering technologies have the potential to offer interesting tools for *in vitro* cell culturing as they allow mimicking of physiologically relevant *in vivo* microenvironments. Research areas in the field of biology, such as stem cell research and so-called organ-on-a-chip microdevices, could benefit greatly from these emerging technologies. In this section, a brief overview of the opportunities for stretchable bioelectronics and within the field of stem cell research will be given. Organ-on-a-chip microdevices have been the subject of recently published review papers, and will not be discussed here [51, 52].

1.2.1 Stretchable bioelectronics

Electrodes establish the link between bioelectrical signals and electronic systems. They have been used for decades for the intra- and extracellular recording and stimulation of electrogenic (= electrically active) tissue and cell cultures, i.e. cen-



(a) (b) Zoomed view of electrode region.

Figure 1.8: Commercially available microelectrode array from Multi Channel Systems MCS GmbH with 60 electrodes [53].

tral and peripheral neurons, heart cells and muscle cells. Multiple microelectrodes can be combined to form microelectrode arrays (MEAs), allowing the simultaneous stimulation and recording of cellular activity at multiple locations in the cell culture or tissue.

Most of today's two-dimensional, planar MEAs are based on glass substrates of approximately 5 cm by 5 cm, which contain electrical conductors and microelectrodes made of various materials (e.g. titanium, platinum, indium tin oxide or gold), passivated by an insulation material (e.g. silicon nitride, silicon oxide, polyimide or SU-8). Openings in the passivation layer define the recording / stimulation sites, of which the number can range from less than 10 to over 100, and are used for non-invasive, extracellular recording / stimulation. An example of a rigid MEA containing 60 electrodes, offered commercially by Multi Channel Systems MCS GmbH, is illustrated in Figure 1.8 [53]. The number and spatial layout of the recording / stimulation sites can typically be customized and provide a means to gather information about interactions between electrogenic cells at different locations in the same culture or tissue. Moreover, cells and tissues are cultured directly on the MEAs, enabling long-term measurements which are essential to e.g. drug response testing.

More advanced applications such as retinal and cochlear implants, deep brain stimulators or brain-computer interfaces require MEAs which can conform to the physical environment and have a reduced mechanical mismatch with the surrounding biological tissue. It was shown that the latter can result in adverse tissue reaction upon implantation [54]. Therefore, MEAs composed of flexible materials such as polyimide [55, 56] or SU-8 [57] have been reported. Although,

the Young's modulus of typical flexible materials such as polyimide (~3 GPa [56]) and SU-8 (~2 GPa [58]) is much lower than that of silicon (~160 GPa [59, 60]), it is still several orders of magnitude higher than that of soft biological tissue (~100 Pa - 100 kPa [61]).
It might not be a surprise that recently, MEAs based on soft, compliant, stretchable materials have been reported as they could conform better to the physical environment and offer a closer mechanical match with the biological tissue [62, 63]. The Young's modulus of e.g. polydimethylsiloxane (PDMS) depends on the fabrication conditions; values in between 50 kPa and 4 MPa have been reported [64, 65]. Furthermore, stretchable MEAs (SMEAs) offer the unique possibility to perform simultaneous electrical and mechanical actuation and monitoring of tissues and cell cultures. They can therefore be used as a research tool to study traumatic brain injury [66, 67], stem cell differentiation [68, 69], etc.

1.2.2 Stem cell research

Stem cells are unique cells which exhibit the potential to either self-renew and maintain the undifferentiated state, or to differentiate in multiple cell types. The *in vivo* microenvironment stem cells reside in, i.e. the stem cell niche, is constituted by specific cell types in a cell-architectural setting. The microenvironment is complex and includes locally produced proteins (including growth factors), cell-matrix interactions and cell-cell interactions, as well as physico-chemical properties such as pH, temperature and oxygen tension. These elements give the environment a distinct physiological character and provide extracellular cues that work together to regulate cell structure, function and behavior [70].
The local *in vivo* microenvironment plays an important role in stem cell differentiation and self-renewal. As shown in Figure 1.9, several physical factors such as fluidic shear stress, mechanical strains and electrical fields are widely believed to regulate stem cell behavior [68]. Microengineering technologies offer the potential to assist stem cell research by mimicking physiologically relevant microenvironments which allow the modulation of different of these factors. Ghafar-Zadeh et al. reviewed engineered microdevices that use microfluidic, mechanical, electrical, optical, magnetic and thermal stimuli for stem cell-based cardiac tissue engineering [68].
Microfluidic technologies have been applied for various purposes such as high-throughput screening, the reduction of culture volumes to limit the consumption of costly reagents or the close control over the spatial and temporal distribution of media content. Precise volumes of media can be delivered at the cellular or subcellular level, stable or time-varying gradients can be generated to realize various reagent concentrations, etc. Chung et al. for example generated gradients of growth factors to optimize neural stem cell proliferation and differentiation [71].
Of specific interest within stem cell research is also the ability to closely control the perfusion of medium and the shear stress exerted at the walls of microfluidic

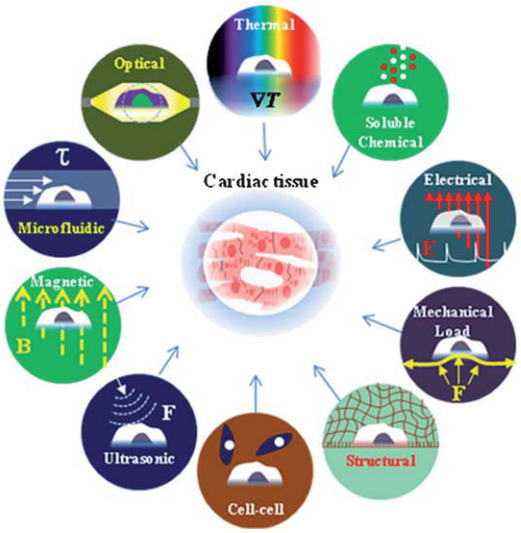


Figure 1.9: Several physical factors have been studied for stem cell-based cardiac tissue engineering [68].

channels. Shear stress for example has been shown to direct stem cell differentiation towards specific cell types such as endothelial and cardiac cells [72–74].

Mechanical forces are typically applied by culturing cells on elastomeric membranes (e.g. silicone membranes). These membranes are subsequently deformed by transducers which are able to modulate the deformation amplitude and frequency. Systems have been designed to exert uniaxial, biaxial or equiaxial strains to cells. Flexcell® International Corporation introduced UniFlex™ and BioFlex® culture plates to apply uniaxial and equibiaxial strains, respectively, to monolayer cell cultures [75, 76]. The working principle is depicted in Figure 1.10: a rubber membrane is deformed across the planar face of a loading post by applying a vacuum beneath the membrane. Smart design of the loading post allows uniaxial and equibiaxial straining of the membrane. Such systems have for example been used to cyclically uniaxially or equiaxially strain stem cells to promote differentiation towards cardiac cells [77, 78]

Electrical stimulation has been shown to promote cell alignment, cell coupling and the amplitude of synchronous construct contractions during the growth of cardiac constructs [79]. Rigid or flexible planar microelectrode arrays (MEAs), as described in Section 1.2.1 and illustrated in Figure 1.8, are the state-of-the-art technology to study the interaction between cells and electrical stimulation / recording *in vitro*. These have been a helpful tool in cell physiological research and drug screening for over a decade. MEAs in particular have been used e.g. to

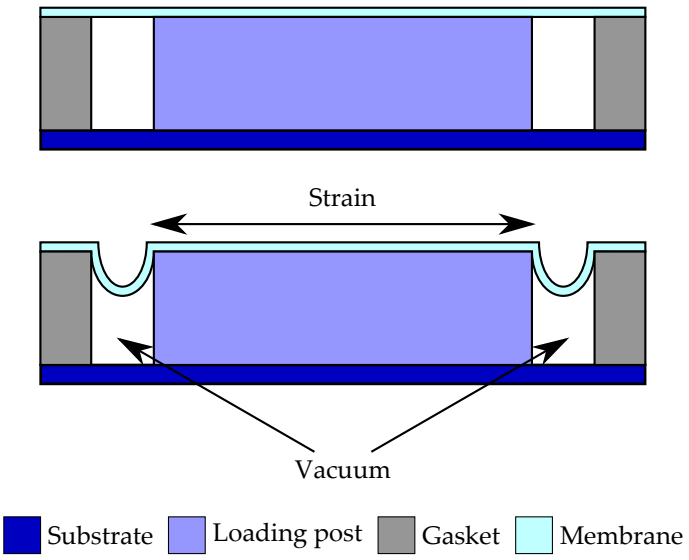


Figure 1.10: Working principle of UniFlex™ and BioFlex® culture plates: a rubber membrane is deformed across the planar face of a loading post by applying a vacuum beneath the membrane.

evaluate stem cell differentiation by electrical recording or to enhance stem cell differentiation towards e.g. cardiac cells by electrical stimulation [80–82].
In addition to the above-mentioned stimuli, also optical, magnetic and thermal stimuli are believed to be relevant for stem cell research, both directly (e.g. direct optical and magnetic stimulation) and indirectly (e.g. by applying mechanical stimuli through optical and magnetic techniques) [68]. However, the utilization of these techniques in the context of stem cell research has been studied less.
It is thus widely believed that diverse stimuli significantly contribute to the culturing and differentiation of stem cells. Hence, there is an obvious need for platforms which allow investigation of the role of the diverse stimuli in these processes separately, but also simultaneously (as is the case *in vivo*). So-called multi-variable platforms will help elucidate the effects of the diverse stimuli by recreating the precise combination(s) of stimuli operative in the stem cell niche. Platforms which allow for the simultaneous application of mechanical strains and electrical recording / stimulation, while allowing the cells to reside in a well-controlled physiologically relevant environment are thus of specific interest.

1.3 Scope and goals

From this introductory chapter, it is clear that electronic circuits which can fully conform and dynamically adapt to arbitrary curved surface topologies have a high potential for being the key enablers for many new applications in diverse areas. The currently presented strategies are, however, disparate and are developed considering a specific target application. This makes them unsuitable for general adoption and a rapid dissemination across disciplines, as the research effort has to be repeated for each development. Furthermore, no attention has been spent on the dual integration of stretchable electronics and microfluidics. Therefore, the goal of this doctoral research consists in the development of a generic technology platform which enables the integration of microelectronics and microfluidics on stretchable substrates, eliminating the drawbacks mentioned above. In order to achieve this goal, several subgoals were defined.
The first subgoal consists in developing electrical interconnections which are able to cope with relatively large mechanical strains without compromising their functionality. From the envisioned applications for the technology platform, the applications requiring continuous stretching, such as the stretchable microelectrode arrays, lead to the most stringent requirements [68]. Strains up to 20 % are targeted, as this value is commonly encountered in the practical applications. The strain is applied at rates varying from 0.1 Hz to 1 Hz, for periods ranging from a few days up to a couple of weeks. Lifetimes in the order of 10^5 to 10^6 straining cycles are therefore targeted. In this context, it is also noted that the developed stretchable electrical interconnections should conform to a reasonable standard of usability in terms of electrical performance. The basic technology for this will be

interconnections based on coplanar metallic spring structures, as this is a proven technology with confirmed results. It also allows relying on prior research conducted within the CMST research group.
A second subgoal consists in combining the stretchable electrical interconnections with functional ICs in order to allow for conformable, stretchable electronics. Although the combination with functional ICs can be achieved in several ways (e.g. assembly using conventional methods based on solder joints or conductive adhesives), the focus will be put on embedding silicon chips as thinned dies. This path offers the greatest flexibility to integrate chips from various manufacturers, while maintaining good overall mechanical flexibility of the electronic system. Therefore, minimum achievable metallization pitches in the order of 50 µm are set as target, exceeding the requirements for interconnection pitches of conventional, commercially available dies.
The third subgoal consists in the development of PDMS-based microfluidics. The technology should not limit the amount of fluidic layers, and allow for the integration of foreign materials. In particular, the integration with porous membranes and microelectronics is investigated.
Complementary to the above-mentioned, specific subgoals, a number of aspects of a more general nature are considered throughout the development of the technology platform.

- A modular approach is striven for, both for the stretchable electronics and the microfluidics. This allows them to be fabricated separately without influencing each other, and to be combined only in the final stage.
- Materials which are known to be cytotoxic are avoided. This is an important aspect considering the amount of biomedical applications.
- Evaluation procedures for all individual modules are set up at each stage to maintain functionality throughout the life span.
- Care is taken to keep all processing steps compatible with conventional equipment for microelectronics processing.

1.4 Outline of this dissertation

Chapter 2 starts by introducing the concept for realizing conformable, stretchable electronics pursued in this dissertation. Next, an overview of microfluidic technologies with specific attention for PDMS-based microfluidics is given. The chapter concludes with an engineering review on the materials which are used for the realization of a stretchable package. Several of the materials such as the metallic conductors, the type of polyimide and the diverse silicone elastomers are presented and their properties are discussed in detail.

Chapter 3 deals with the fabrication and evaluation of thin-film stretchable electrical interconnections. Special attention is given to improve the lifetime during cyclic mechanical loading. These interconnections are then used to build the stretchable electronics platform using thin dies, presented in Chapter 4. The process is developed with so-called daisy chain silicon dies, which allow for quantification of the contacting yield from the package to the die level.
In Chapter 5, single- and multi-layer PDMS-based microfluidics are described. Micropatterning of PDMS is performed via replica molding using photolithographically defined SU-8 master molds. Furthermore, the integration of membranes and the combination with the electronics platform presented in Chapter 4 is illustrated.
A number of applications enabled by and benefiting from the technologies which are presented in Chapter 3, Chapter 4 and Chapter 5 are highlighted in Chapter 6. Both elastic microsystems with modular functionalities and PDMS-based microfluidics for cell culturing are discussed. Focus is put on the developments and the initial results achieved within the IWT-SBO funded projects 'BrainSTAR' and 'HEPSTEM', respectively. Finally, Chapter 7 concludes this dissertation by summarizing the main achievements of this work and recommending some interesting topics for future research.

1.5 Research dissemination

Papers published in an SCI-journal

- R. Verplancke, F. Bossuyt, D. Cuypers, and J. Vanfleteren, "Thin-film stretchable electronics technology based on meandering interconnections: fabrication and mechanical performance," *Journal of Micromechanics and Microengineering*, vol. 22, no. 1, p. 015002, Jan. 2012.

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2
Concepts and materials

2.1 Introduction

In the introductory chapter, a thorough overview is provided of the state-of-the-art of stretchable electronics. Furthermore, it is highlighted that the possibility to combine stretchable electronics with microfluidics can improve applications in health care or boost research in the field of microbiology. On the one hand, one could imagine devices that regulate drug or insulin delivery after *in situ* analysis of the blood. Such devices would desirably be unobtrusive, conformable, compact and lightweight. Within the field of stem cell research, on the other hand, there is an obvious need for so-called multi-variable platforms which allow for the simultaneous application of mechanical strains and electrical recording / stimulation, while allowing the cells to reside in a well-controlled physiologically relevant environment. The goal of this doctoral research is to develop a generic technology platform in order to comply with the requirements of such devices and multi-variable platforms. Stretchable electronics and microfluidics are considered to be the main building blocks; some basic concepts and the various materials are introduced in this chapter.
In the first section of this chapter, the concept for realizing conformable, stretchable electronics pursued in this dissertation is presented. Meandering horseshoe shaped metallic conductors and thinning of dies are described in detail as these form the basis for the realization of the concept. In the next section, microfluidic technologies are introduced: traditional and soft-lithographic techniques to micropattern PDMS are reviewed. The remainder of the chapter deals with several

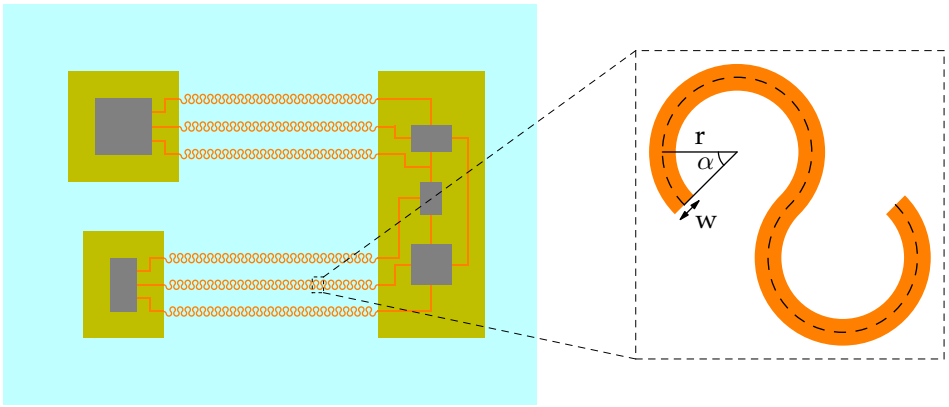


Figure 2.1: A pixelated architecture for stretchable electronics: various non-stretchable islands are connected by stretchable electrical wiring.

of the materials, such as the metallic conductors, the type of polyimide and the diverse silicone elastomers. In addition, a brief overview of their properties is presented.

2.2 Stretchable electronics

As mentioned in Chapter 1, two-dimensional meandering metallic conductors form the basis of the stretchable electronics platform described in this dissertation. This section will cover the basic concepts.

2.2.1 System architecture

A general concept for realizing conformable, stretchable electronics consists in the use of a pixelated architecture fixated on an elastomeric substrate: various non-stretchable islands are connected by stretchable electrical wiring, which is able to deform with the elastomeric substrate. This architecture is illustrated in Figure 2.1.
The islands are composed of a structural polymer, and are designed to host fragile devices and protect them from large deformations. Traditional, rigid electronic components such as sensors, actuators and their conditioning electronics are thus mounted on the islands and are interconnected in a conventional way. It is clear that in order to improve the overall flexibility and conformability, a certain degree of flexibility in the islands is also desired. To achieve this, unpackaged active components can be thinned and embedded in the structural polymer.

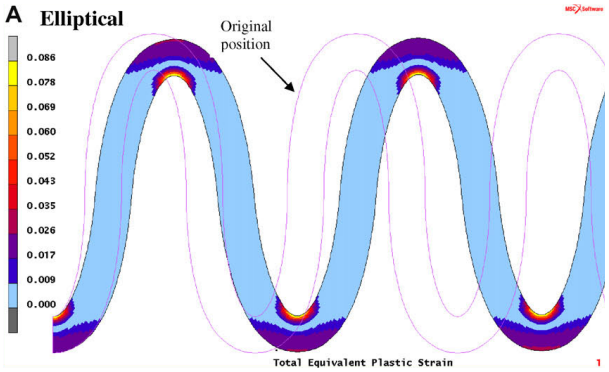
2.2.2 Stretchable electrical interconnections

Stretchable electrical interconnections form a key challenge to enable stretchable electronics, as they should be able to deform with the elastomeric substrate without compromising the electrical performance. They are realized by meandering metallic conductors that are able to function as 'two-dimensional springs' when embedded in an elastomeric substrate. A reliable design is essential to ensure the functionality during extreme and repeated deformations.

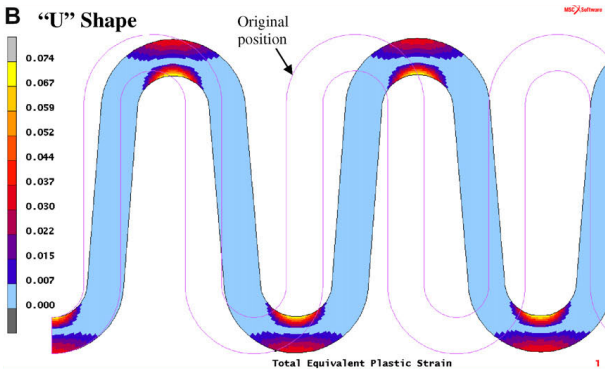
Intuitively, it is expected that metallic conductors composed of a repetitive triangular or sinusoidal unit allow for higher deformations than straight lines. However, these shapes can still present high stress concentrations in certain regions, resulting in failures at moderate deformations. As a first step towards optimization of the repetitive unit, finite element modeling was used to compare the performance of different shapes. Gonzalez et al. compared stresses in patterned copper conductors subjected to 20 % strain in the axial direction [1]. Three different shapes were compared: an elliptical, "U" and horseshoe shape. The conductor thickness, width, shape amplitude and period were fixed at 15 µm, 90 µm, 700 µm and 500 µm, respectively. The effect of the elastomeric substrate was ignored, as well as the out of plane deformation of the metallic conductor. The latter was justified by noting that full embedding of the metallic conductor in an elastomeric substrate constrains the out of plane deformation.

The elliptical shape (Figure 2.2(a)) was found to suffer from high stress and strain concentrations in the crests and troughs of the conductor. To improve the stress distribution, a higher radius of curvature is desired and the "U" shape (Figure 2.2(b)) was proposed. Although the latter effectively offers a better stress distribution, the radius of curvature is still limited. Furthermore, the straight vertical lines limit the deformation perpendicular to the axial direction (e.g. due to the Poisson's effect). Therefore, the horseshoe shape (Figure 2.2(c)) was proposed and was found to result in a better stress distribution over an extended part of the conductor. Compared to the elliptical shape, the equivalent plastic strain, which determines when the metal will start cracking or break, was reduced by 39.2 % for an identical elongation.

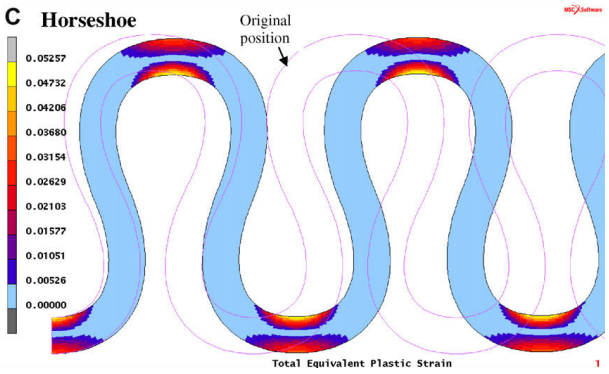
Based on this rudimentary comparison of different shapes, the horseshoe shape was chosen as repetitive unit. Nevertheless, the actual stress magnitudes are related to several factors such as the elongation, the geometry of the horseshoe shape, the stiffness of the elastomeric substrate and the interconnection pitch. This has been extensively investigated through both numerical simulation and experimental investigation, and has been the topic of several papers [1–7]. It should be noted that, although the metallic conductors in these papers were assumed to be copper, the general trends are also valid for horseshoe shapes composed of other materials. In what follows, the most important findings will be summarized; the reader is referred to the corresponding papers for more information.



(a) Elliptical shape.



(b) "U" shape.



(c) Horseshoe shape.

Figure 2.2: Distribution of equivalent plastic strain in meandering copper conductors for three different shapes of the repetitive unit [1].

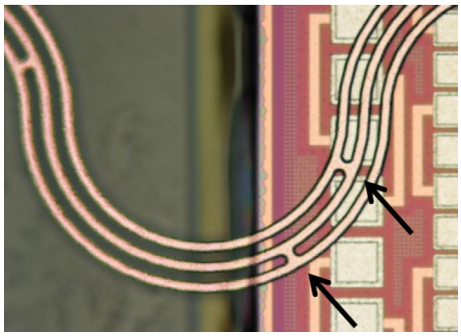


Figure 2.3: Bridges in between parallel, fine-line horseshoe shaped tracks [6].

The mechanical design parameters, angle α, radius r and width w, are indicated in Figure 2.1. By properly designing the horseshoe shapes, the local strain magnitudes in the conductor can be further reduced to stay well below the point of rupture. Gonzalez et al. reported that designs with an identical scale factor $\frac{r_{in}}{w}$, r_{in} being the inner radius of the horseshoe shape and w the conductor width (Figure 2.1), result in an identical stress and strain in the metallic conductor [1]. Increasing the scale factor, by reducing the conductor width or increasing the amplitude, reduces the induced strain and is therefore preferred. However, the design is determined by various factors such as the applied deformation, track resistance and interconnection pitch. It is clear that increasing the amplitude or reducing the conductor width will result in a larger track resistance. Furthermore, increasing the amplitude also limits the interconnection pitch.

In order to exploit the reduced stress magnitudes of a fine-line metallization scheme without compromising the electrical conductivity, multiple horseshoe shaped tracks can be designed parallel to each other [1, 6]. By including bridges between the parallel tracks in the regions where the lowest deformation is observed, only a small section of the metallic conductors is lost upon failure of one of the parallel tracks, i.e. the section in between two adjacent bridges. This is illustrated in Figure 2.3. The redundancy thus helps to increase the reliability of the stretchable interconnections.

Gonzalez et al. also illustrated the effects of the substrate material on the strains induced in the metallic conductor [1, 2]. It was found that substrate materials with low Young's modulus are preferred, as they allow for larger deformations without permanent damage (smaller plastic strain) in the metallic conductor. This is explained by noting that in case a substrate with high Young's modulus is used, the deformation of the metallic conductor is completely imposed by the substrate, whereas a substrate with low Young's modulus allows for local diminishing of the strain close to the metallic conductor. Hsu et al. analyzed the effects

of encapsulation on the deformation behavior and failure mechanisms of horseshoe shaped stretchable interconnections [3]. It was shown that encapsulating the stretchable interconnections limits the out of plane deformation and alters the in plane geometrical opening during stretching. As the thickness of the encapsulation layer increases, the effects are more pronounced and result in larger plastic strains in the metallic conductors.
Practical applications typically require multiple signal paths which often have to be designed parallel to each other. The pitch was also found to have an effect on the deformation and failure of the horseshoe shaped interconnections [5]. It was reported that the plastic strain can drop drastically by increasing the pitch. Often, a trade-off imposes itself as it is clear that the pitch is determined by the available space for routing.
Experimentally, the failure mechanisms of horseshoe shaped metallic conductors were observed to be crack formation and crack propagation, similar to fatigue fracturing [4, 8]. Generally, a distinction is made between low-cycle and high-cycle fatigue. The former occurs when stresses are large enough for plastic deformation to occur, resulting in a relatively small number of cycles before failure. High-cycle fatigue, on the other hand, occurs when stresses are small and deformations elastic, resulting in a high number of cycles before failure.
As mentioned above, the formation of cracks can be postponed by a number of measures which tremendously decrease the magnitude of the stress levels in the metallic conductor. The crack propagation on the other hand can be delayed by introducing a polymer material with a higher Young's modulus than PDMS as a support for the horseshoe shaped metallic conductors; the support material is patterned in a similar shape as the metallic conductors. Polyimide was suggested as a support material as it is a common material in electronics industry and ideally suited for this purpose (see Section 2.4.2). Furthermore, proper design of the polyimide support can effectively reduce the plastic strain in the metallic conductor, e.g. by increasing the polyimide width or thickness, again postponing the formation of cracks [7]. This will be experimentally verified in Chapter 3.

2.2.3 Thin dies

Standard silicon wafers have diameters ranging from 25.4 mm to 300 mm. The wafer thickness is dependent on the wafer diameter and increases steadily with increasing wafer diameter, reaching 775 µm at a wafer diameter of 300 mm. This ensures mechanical and thermal stability during the wafer and device manufacturing, without neglecting affordability (bulk silicon cost). Furthermore, the wafer thickness is standardized to enable equipment compatibility and automation.
Dies (or chips) thus have a thickness which is dependent on the original wafer diameter, and can easily measure several hundred micrometers. Thin dies are however an enabler for various emerging applications where minimum die thickness,

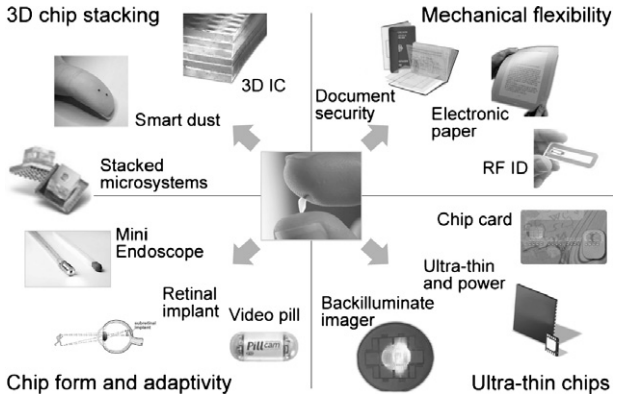


Figure 2.4: Various emerging applications benefit from thin dies [9].

die flexibility or non-planar assembly is required [9]. Figure 2.4 illustrates several examples. Ultrathin dies are of interest for form factor reasons e.g. in smart cards, or to improve the power dissipation to the package by reduced thermal resistance. Biomedical applications such as retinal implants benefit from dies which can adapt to the shape of the retina and which have minimum overall dimensions. Driver chips in flexible displays and RFID tags exploit mechanical flexibility to support mechanical reliability or bendability. Furthermore, 3-D chip stacking enables compact microsystems. In combination with dense through-silicon via (TSV) processes, this is considered an enabler on the international technology road map for semiconductors (ITRS) (cf. interconnect bottleneck) [10].

Flexibility

Mechanical flexibility by thinning exploits an elementary result in mechanics: common electronic materials, or any material for that matter, become flexible if sufficiently thinned. This is easily explained by noting that the magnitude of the bending strains and corresponding stresses is greatly reduced as the thickness decreases. To illustrate this, consider a beam of homogeneous material subject to the bending moments depicted in Figure 2.5. Assume that (a) the cross section of the beam is symmetrical about an axis perpendicular to the neutral surface and (b) all cross sections of the beam remain plane and perpendicular to the longitudinal axis during the deformation. The normal strain ϵ of any element within the beam can then be determined as [11]:

$$\epsilon = -\frac{y}{\rho} \tag{2.1}$$

This indicates that the normal strain ϵ depends both on the location y on the cross

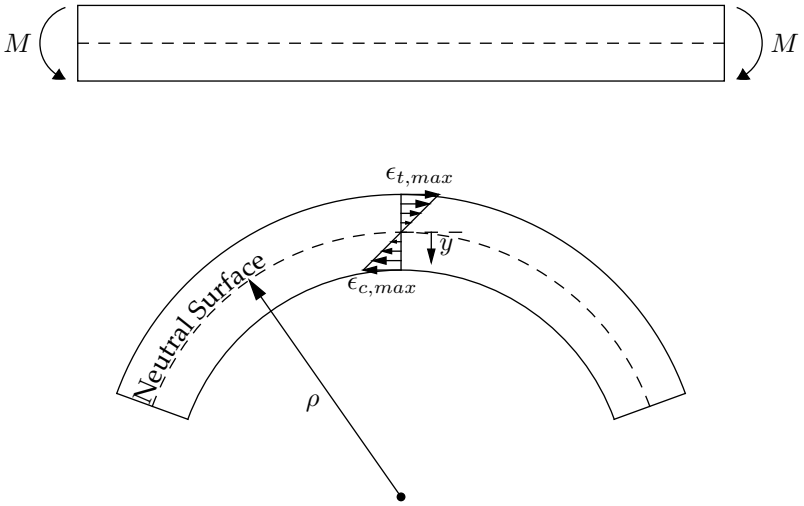


Figure 2.5: Strain distribution in a beam subject to bending moments.

section and the radius of curvature ρ of the beam's longitudinal axis, and varies linearly across the cross-sectional surface. Consequently, the bending moment will cause a maximum tensile strain in the outer surface at the convex side and a maximum compressive strain in the outer surface at the concave side. Furthermore, this implies that between the tensile and compressive region there is a surface, called the neutral surface, in which the longitudinal fibers of the material are not strained. It is clear that by decreasing the thickness of the beam, both the maximum tensile and compressive strain are reduced. Assuming that the material behaves in a linear-elastic manner so that Hooke's law applies, i.e. $\sigma = E\epsilon$ with E the material's Young's modulus, a similar conclusion can be made for the normal stress σ.

Thinning

The thinning of dies can be performed either on wafer-scale or individually, to the thicknesses mentioned in Table 2.1. Obviously, both techniques have their unique advantages. Individual dies are thinned if a limited number of thin dies is required (e.g. for research purposes), to avoid the handling of fragile thin wafers or simply because no full wafers of the specific die are available. Wafer-scale thinning on the other hand is more cost-effective when larger numbers of thin dies are required. The dies used in this thesis, i.e. the PTCE silicon die and the microcontroller MSP430F1611, were thinned on wafer-scale.
The conventional technique to provide thin wafers is wafer back-thinning. Dur-

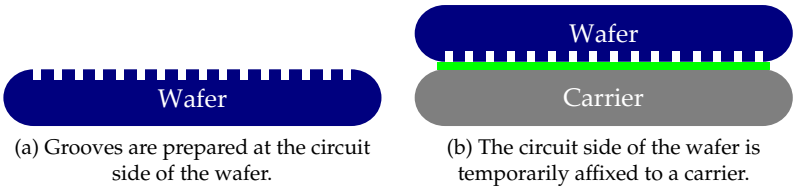
Thickness range	Mechanical properties
> 300 µm	Unconditional mechanical stability
100 µm - 300 µm	Stiffness but limited mechanical stability
50 µm - 100 µm	Limited stiffness and limited mechanical stability
10 µm - 50 µm	Good flexibility and good mechanical stability
< 10 µm	Excellent flexibility and unconditional mechanical stability

Table 2.1: Ranges of wafer thickness and corresponding mechanical properties [10].

ing device manufacturing, the wafer thickness is left untouched to ensure mechanical stability and stiffness during (automated) wafer handling. The wafer is subsequently thinned to the desired thickness. Mechanical grinding is the most common wafer thinning technique because of its high thinning rate, and is typically composed of a coarse and fine grinding step. The latter step is required to remove most of the damage and to reduce the surface roughness introduced by the coarse grinding, as these cause stress in the thinned wafer and make them fragile.

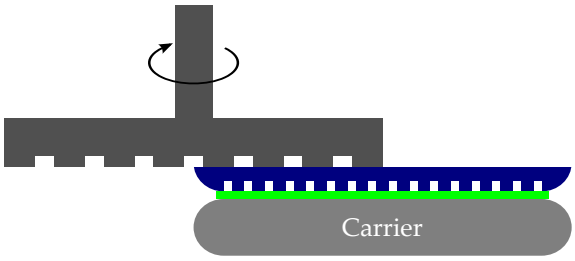
The ranges of wafer thickness and corresponding mechanical properties are summarized in Table 2.1 [10]. Note that the mechanical stability has to be interpreted as the susceptibility to fracturing. It is clear that at such small thicknesses, the wafers are very fragile. Rough surfaces or edges for example can induce fracture due to stress maximums, especially at the lower thickness range. Therefore, additional efforts are required in order to achieve better surface planarization, edge smoothing and stress relief. To this end, either chemical mechanical polishing (CMP), wet etching and / or dry etching can be applied.

Separating wafers into dies is most commonly performed using sawing equipment running diamond blades. However, conventional wafer dicing induces crystalline defects and microcracks at the sidewall of the dies, which become a serious problem with thin wafers. Therefore, new techniques such as dicing by thinning (DbyT) or dicing before grinding (DBG) have been developed. The concept of DbyT is simple: grooves are prepared at the circuit side of the wafer (e.g. by half-cutting or dry etching), the wafer is temporarily affixed to a carrier and subsequently backside thinning is performed until the front grooves are reached. This concept allows for a variety of adaptations and variations, and offers several advantages: die edges may have any form (in particular when dry etching is performed to prepare the grooves), sidewalls of dies show no mechanical damage, outer dimensions of dies are quite uniform, dicing of a complete wafer is less time-consuming, etc. More importantly, the concept has been shown to improve the die strength [10].



(a) Grooves are prepared at the circuit side of the wafer.

(b) The circuit side of the wafer is temporarily affixed to a carrier.



(c) Backside thinning is performed until the front grooves are reached.

(d) Separated dies are attached to the carrier upon successful dicing.

Figure 2.6: Dicing by thinning concept.

Additional processing, assembly and embedding

Often, the thin dies require additional processing: metal pads are surface finished, partial or complete encapsulation is performed, backside metallization is applied, etc. Furthermore, to assemble and embed the thin dies, they have to be picked up, transferred and placed. These steps are not straightforward and have to be performed with great care: warpage can introduce aligning errors and can be worsened by additional processing, dies can bend or crack during pickup and placement, etc. In this dissertation, pickup, transfer and placement of the thin dies is performed manually, while additional processing is performed when the die is fixated on the substrate.

2.3 Microfluidic technologies

In its early stages, microfluidics benefited greatly from microfabrication technologies developed for semiconductors by the microelectronics industry: photolithography and etching techniques developed for silicon and glass were used to fabricate the first microfluidic devices, as these techniques were available, well established and precise. However, the production of silicon or glass microfluidic devices is generally expensive and time-consuming, and requires access to cleanroom facilities. Consequently, their use in research requiring rapid evaluation of prototypes is limited, and there has been a gradual shift towards alternative, cheaper materials and techniques. The focus hence shifted towards polymers such as poly(methyl methacrylate) (PMMA), polycarbonate, polyimide, SU-8 or PDMS, and techniques such as laser ablation, hot embossing, injection molding or replica molding [12]. Due to the large variability in polymers and corresponding mechanical and chemical properties, microfluidic technologies have also become more versatile.
Although various polymers have become popular in the field of microfluidics, PDMS in particular is highlighted as it really has boosted research due to its low cost and ease of use. Soft-lithographic techniques are used to replicate the relief structures present on the surface of a mold; these techniques allow for rapid prototyping, do not require cleanroom facilities and benefit greatly from the flexibility of PDMS. Furthermore, PDMS exhibits several favorable properties that make it suitable for microfluidic devices for a wide variety of applications. Optical transparency enables optical detection at a wide range of wavelengths ranging from near-infrared down to near-UV. The high permeability to gases allows the filling of dead end channels, but also allows the exchange of gases (e.g. oxygen) for cell cultures in closed systems [13, 14]. Biocompatible types of PDMS are commercially available to support biomedical applications. The elasticity enables the integration of different fluidic components such as valves and pumps [15]. Its surface properties allow both for reversible and irreversible sealing [16]. Reversible sealing to various materials such as glass, silicon and plastics occurs

because PDMS conformally contacts smooth surfaces; irreversible sealing to certain materials can be obtained after surface modification by exposure to an oxygen or air plasma (Section 5.2.4).
In what follows, an overview will be given of the different techniques which can be employed to micropattern PDMS. A distinction is made between traditional techniques such as wet and dry etching, which selectively remove parts of a layer of PDMS, and soft-lithographic techniques.

2.3.1 Traditional techniques to pattern PDMS

Photolithography

The vast majority of the available PDMS materials cannot be patterned directly using photolithography. The WL-5000 series from Dow Corning, however, are a series of photosensitive PDMS materials which are patterned in a conceptually similar way as negative photoresists [17, 18]. In addition, several papers have been published which report on the custom synthesis of photosensitive PDMS by the addition of UV-sensitive photoinitiators or photoinhibitors [19–25]. However, it is clear that this process is not straightforward. Furthermore, several of these photosensitive PDMS materials have a limited resolution and exhibit altered mechanical properties compared to the non-modified materials.

Wet etching

Wet etching is typically performed by applying a masking material and removing the target material in the areas exposed to the etchant. As PDMS is relatively inert to many chemicals, this method has been proven to be quite hard. Several papers have reported on the selective removal of PDMS using a solution of tetrabutylammonium fluoride ($C_{16}H_{36}FN$) in n-methyl-2-pyrrolidone (C_5H_9NO) in a 1:3 volume mixing ratio [26–29]. However, no encouraging results were obtained: high surface roughnesses were observed, while the precision was limited due to the high isotropy and failure of the aluminium masking layers.

Dry etching

As is the case with wet etching, a masking material is applied and the target material is removed in the areas exposed to the generated plasma. Dry etching conditions typically depend on the etch tool, and can be optimized in terms of e.g. etch speed, selectivity or surface roughness. Oxygen plasmas, commonly used for polymer etching, were reported to convert the PDMS surface into a SiO_x-like material, and result in very small etch rates [30]. Various other dry etch recipes are based on oxygen plasmas with a fluorine containing source gas such as CF_4 [27–29, 31] or SF_6 [32]. Careful process optimization is required while these processes generally result in long etch times and large surface roughnesses.

Furthermore, dry etching of PDMS requires the availability of a dedicated set-up to avoid cross-contamination of other processes (Section 2.4.3).

Laser ablation

In contrast to the other traditional techniques, laser ablation does not require photolithography. The material to be patterned is exposed to high-power incident radiation, resulting in the removal and ejection of ablated material through photochemical (UV) and photothermal (IR) processes. The exact mechanism depends on the radiation wavelength and the material properties. Both processes have been reported in this context by patterning PDMS using CO_2 (9 µm - 11 µm), KrF excimer (248 nm) and frequency-quadrupled Nd-YAG lasers (266 nm) [28, 33–35]. These procedures require the optimization of various parameters (e.g. laser power, speed and pulse frequency), but generally do not result in a satisfying ablation procedure. Furthermore, one has to consider the minimum achievable feature sizes, re-deposition of the ablation products (debris), but also the ablation selectivity.

2.3.2 Soft-lithography

Soft-lithography denotes a set of fabrication techniques used to fabricate or replicate structures using elastomeric stamps, molds and conformable photomasks [36]. As these techniques rely on molding and replication instead of patterning and etching, they provide a convenient, non-photolithographic, low-cost strategy for micro- and nanofabrication. Furthermore, they offer advantages in a number of applications such as patterning of solid materials other than photoresists, patterning of liquid materials, patterning on non-planar surfaces, etc.
Various techniques such as replica molding (REM), microcontact printing (μCP), microtransfer molding (μTM), micromolding in capillaries (MIMIC) and solvent-assisted micromolding (SAMIM) have already been explored [37]. The key aspect is an elastomeric block with patterned relief structures on its surface, fabricated by replicating the three-dimensional topography of a patterned, solid surface, also called the master mold. This is done by a sequence of casting, curing and peeling. The master mold on the other hand is fabricated using traditional microfabrication techniques such as photolithography or micromachining. Because master molds are typically rigid, using an elastomer (e.g. PDMS or polyurethane) facilitates peeling off the replica.

Replica molding

Replica molding (Figure 2.7) is a simple but efficient method to replicate the relief structures present on the surface of a mold. A liquid prepolymer is cast and cured on a mold, and subsequently peeled off. Using elastomeric molds rather than rigid molds facilitates the release of small, fragile structures.

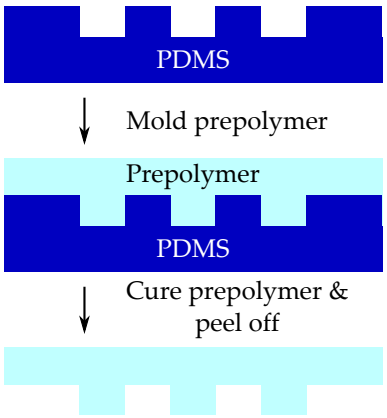


Figure 2.7: Schematic illustration of replica molding.

Microtransfer molding

In microtransfer molding (Figure 2.8(a)), a thin layer of liquid prepolymer is applied to an elastomeric mold and the excess material is removed (e.g. by scraping). The mold is then brought into conformal contact with a substrate, and the liquid prepolymer is cured by heating or UV exposure. Removing the mold results in patterned microstructures on the surface of the substrate. Note that a residual layer is always present; this is indicated in Figure 2.8(a).

Micromolding in capillaries

Micromolding in capillaries (Figure 2.8(b)) is performed by conformally contacting an elastomeric mold with a substrate, while the patterns are facing down. A network of empty channels is formed which is filled by a (low-viscosity) liquid prepolymer. The filling is performed spontaneously by capillary action by placing the liquid prepolymer at the open ends of the channels. Curing the prepolymer and removing the mold results in patterned microstructures on the substrate.

Microcontact printing

Microcontact printing (Figure 2.8(c)) uses the relief structures on the surface of an elastomeric stamp to form patterns of self-assembled monolayers (SAMs) on the surface of a substrate. To this end, the stamp is coated with the material to be patterned and brought into conformal contact with the substrate. Subsequent separation results in patterned layers of material on the substrate.

Solvent-assisted micromolding

Solvent-assisted micromolding (Figure 2.8(d)) creates relief structures in a material (typically an organic polymer). To this end, an elastomeric mold is wet with an appropriate solvent which is able to dissolve or soften the material, and the mold is placed in conformal contact (patterns facing down) with the material. The material is dissolved and fills the structures of the mold. Evaporation of the solvent solidifies the fluid. By removing the mold, a patterned surface of the material is obtained. As is the case with μTM, a residual layer is typically present.
In order to enable a modular approach for the dual integration of stretchable electronics and microfluidics (Section 1.3), replica molding is of particular interest. This technique allows for the straightforward fabrication of well-defined, micropatterned PDMS membranes using a photolithographically defined master mold (Section 5.2.3). The micropatterned PDMS membranes can subsequently be used to create microfluidic channels by bonding them to a suitable, preprocessed base substrate or membrane, as explained in Section 5.2.4.

2.4 Materials

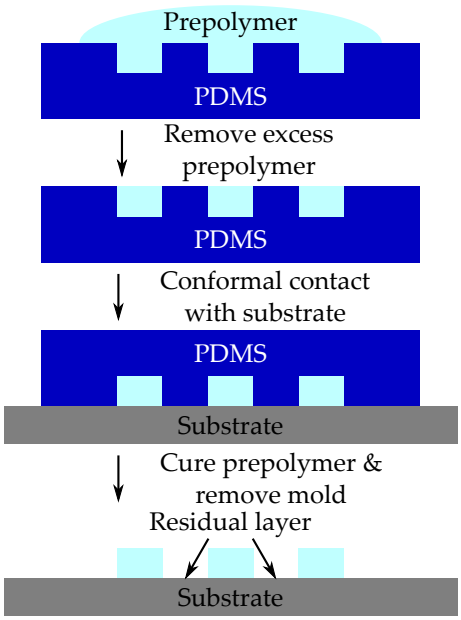
2.4.1 Metallic conductor

Selection

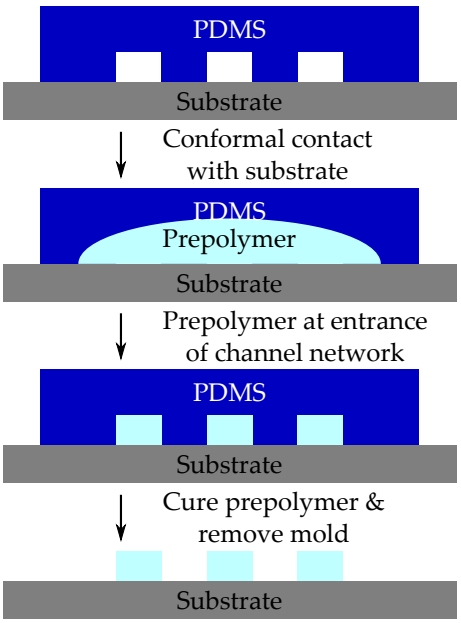
The prime requirements for the metallic conductor are:

- High conductivity: to avoid large voltage drops or large thermal noise.
- Ability to achieve fine-pitch metallization schemes: thin-film metallization is thus required, hence vacuum deposition is the preferred deposition technique. Minimum achievable metallization pitches in the order of 50 µm are set as target, exceeding the requirements for interconnection pitches of conventional, commercially available dies.
- Non-toxicity: to retain the possibility of biomedical applications.
- Compatibility with base materials: during dry etching of polyimide or wet etching of aluminium (see Chapter 3 and Chapter 4), selectivity is required.

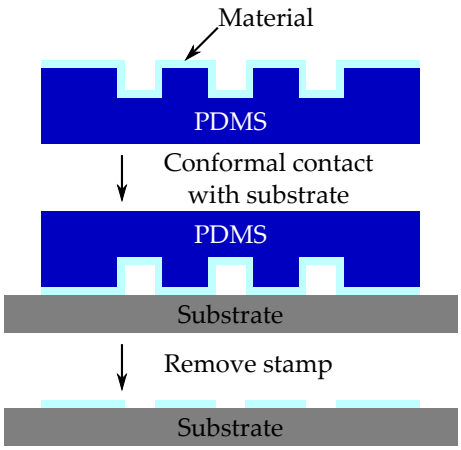
The choice for the metallic conductors is as varied as the range of metals which can be sputter deposited or evaporated. Following metals were considered: copper, aluminium, titanium, gold and platinum. Copper and aluminium are commonly used metals in thin-film processing and have very good electrical properties. However, they were not selected because they are known to be cytotoxic. Titanium on the other hand is known to be non-toxic, but exhibits a rather high electrical resistivity (~25 times larger than copper). Platinum and gold are noble



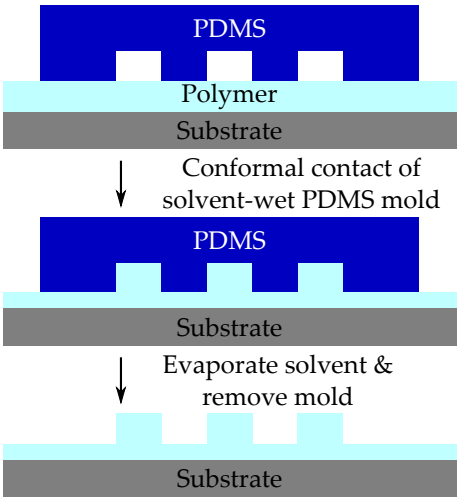
(a) Microtransfer molding (μTM).



(b) Micromolding in capillaries (MIMIC).

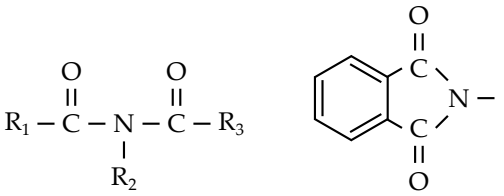


(c) Microcontact printing (μCP).



(d) Solvent-assisted micromolding (SAMIM).

Figure 2.8: Schematic illustration of various soft-lithographic fabrication techniques.



(a) Imide. (b) Phthalimide.

Figure 2.9: Chemical structure of imide and phthalimide.

metals which means that they are resistant to corrosion and oxidation. They are known to be non-toxic and are frequently used in biomedical applications. Platinum was not readily available, is more expensive than gold and exhibits a larger electrical resistivity (~4 times larger than gold). Therefore, gold was chosen as the metallic conductor throughout this dissertation.
Sputter deposition is preferred over evaporation because of its better step coverage and better adhesion to the substrate (in this work polyimide). However, it was found that gold sputter deposited directly on polyimide detaches during processing. Therefore, an adhesion enhancement layer composed of titanium tungsten is sputter deposited in the same vacuum cycle prior to the gold deposition.

2.4.2 Polyimide

Chemistry

Polyimides are long-chain organic polymers of imides, i.e. a functional group consisting of two acyl groups bound to nitrogen (Figure 2.9(a)). Very often, polyimides are characterized by the presence of the phthalimide structure in their backbone (Figure 2.9(b)). The backbone can be more generally represented by the chemical structure displayed in Figure 2.10, with R_1 and R_2 mainly aromatic groups which are responsible for the high thermal stability. Different R_1 and R_2 groups in the backbone are responsible for differing electrical, physical and chemical properties of various polyimides.
To coat thin films of polyimide over a variety of substrates, a two step process is frequently used which involves the application and polymerization of a soluble polyimide precursor. The polyamic acid precursor is dissolved in a solvent carrier such as n-methyl-2-pyrrolidone (NMP), and can be applied by common techniques such as spin coating, spray coating or screen printing. After application, the polyamic acid precursor is converted into the final, insoluble polyimide film by thermal curing or imidization. This process is typically composed of two

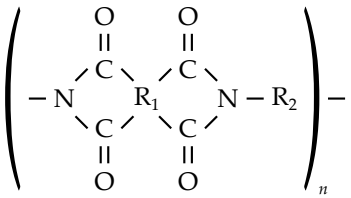


Figure 2.10: General representation of the polyimide backbone.

stages: a soft bake and final cure. The soft bake is performed in air at temperatures ranging from 130 °C to 200 °C, and its main purpose is to drive off the solvent carrier. Imidization may already start at these temperatures. The final cure is performed in an inert (e.g. nitrogen) atmosphere, at temperatures up to 350 °C to achieve complete imidization.

Properties

Polyimide layers have been widely used as dielectric and passivation layers in the microelectronics industry for many years, as they exhibit exceptional electrical, thermal and mechanical properties. Their high electrical resistivity, low dielectric constant and high breakdown voltage make them particularly suitable as insulating layers in multilevel interconnections. Their high thermal stability and superior chemical resistance render them compatible with many processes, and also expand the application space. Furthermore, their favorable mechanical properties such as high tensile strength and high Young's modulus, combined with the flexible nature of polyimides, make them ideally suited for use as substrates in flexible circuits. Such circuits are e.g. found in mobile phones and cameras, where they are used to provide interconnections between rigid boards to allow deformation and / or to save space.
Despite the many attractive properties, some disadvantages are also worth mentioning. First, polyimides are prone to moisture absorption (up to 3 % by weight). The moisture uptake can eventually result in adhesion failure. Furthermore, it is known to alter the electrical and mechanical properties. Second, polyimide is a relatively expensive material.

Selection

A variety of polyimides are commercially available, each with its unique properties. Selection is based on criteria such as the process compatibility and the cured film properties. Process compatibility is determined by several factors such as the patterning technology, curing temperature, planarization properties and adhesion properties. Photodefinable polyimides can be negative tone, solvent pro-

cessed or positive tone, aqueous processed. Standard, non-photodefinable polyimides on the other hand require the use of a photoresist, followed by wet or dry etching. The patterning technology also affects the resolution: photodefinable materials generally have a better resolution than wet etching, while dry etching was found to have the best resolution with very high aspect ratios. Requirements for the cured film are quite diverse; glass transition temperature, CTE and film thickness typically are important selection criteria.
The prime requirements for the polyimide are:

- High resolution patterning: the requirement for a fine-pitch metallization scheme implies that a high resolution patterning of the polyimide is required as the polyimide will be patterned with a similar pitch (see Chapter 3). Dry etching is thus the preferred patterning technique, while the film thickness should be somewhat limited. Feature sizes in the order of 100 µm are set as target.

- Non-toxicity: to retain the possibility of biomedical applications.

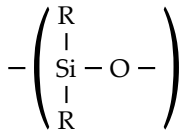
- Low stress: as different layers of polyimide are spin-coated on glass substrates with a CTE of 8.7 ppm $^{\circ}C^{-1}$ [38], a CTE close to that of the glass substrates is preferred to avoid large internal stresses in the polyimide after release.

- Electrically insulating

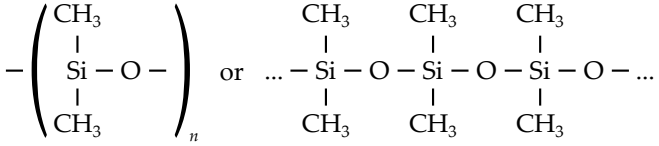
Selection of an appropriate polyimide based on these requirements pointed out PI-2611 from HD Microsystems^{TM} as a suitable polyimide. Although PI-2611 is not classified as biocompatible by HD Microsystems^{TM}, it has been described to be non-toxic in numerous papers. Furthermore, it is a low stress polyimide and has a CTE of 3 ppm $^{\circ}C^{-1}$, which is close to the CTE of the glass substrates (8.7 ppm $^{\circ}C^{-1}$). Film thicknesses in the range of 4 µm to 8 µm can be achieved with a single spin coat process; cured films can be patterned using dry etching. Additional desirable properties are its low moisture uptake (0.5 %) and high Young's modulus (8.5 GPa).

Processing guidelines

Adhesion promoters Frequently, adhesion promoters are required to enhance the adhesion of polyimide to other substrate surfaces (e.g. silicon dioxide, silicon nitride or metals). VM-651 and VM-652 (HD Microsystems^{TM}) are adhesion promoters based on organosilanes and can be used to improve the adhesion of a large class of polyimides to substrate surfaces which form a native oxide.



(a) Siloxane.



(b) Polydimethylsiloxane.

Figure 2.11: The basic repeating unit of silicone, "siloxane", and the most common silicone "polydimethylsiloxane".

2.4.3 Polydimethylsiloxane

Chemistry

Silicones are a class of polymers whose backbone consists of repeating silicon to oxygen bonds. In addition to these bonds, the silicon atoms are also bonded to organic groups (e.g. methyl, vinyl or phenyl). The basic repeating unit is known as "siloxane" and is shown in Figure 2.11(a). The most common silicone is obtained when methyl groups are bonded to the silicon atoms (Figure 2.11(b)), and is known as polydimethylsiloxane (PDMS).
The physical form of the polydimethylsiloxanes range from resins to liquids with varying viscosities. They can be transformed into a three-dimensional network, or an elastomer, by formulation and cross-linking, allowing the formation of covalent bonds between adjacent chains. Different cross-linking reactions can be used: cross-linking with radicals, by condensation or by addition [39–41].

- Cross-linking with radicals is in particular achieved when the silicone polymer carries vinyl groups.
- Cross-linking by condensation is started when the silicone polymers come into contact with moisture, e.g. from the ambient air, and requires no mixing. This type of reaction is commonly found in silicones for the construction industry, but also in silicone adhesives, encapsulants and sealants for medical devices.
- Cross-linking by addition requires the reaction of a vinyl endblocked polymer with Si-H groups carried by a functional oligomer / polymer (or crosslinker), catalyzed by platinum or rhodium metal complexes. If a crosslinker with many Si-H groups is used, a large number of vinyl endblocked

polymer chains can be cross-linked together. Silicone elastomers using this reaction require the mixing of two components. Usually, part A, commonly referred to as the base agent, contains a.o. the vinyl endblocked polymer and the platinum or rhodium catalyst, while part B, commonly referred to as the curing agent, contains a.o. the cross-linkers carrying the Si-H groups. The mixing ratio depends on the type of silicone elastomer, and is specified in the product datasheet. Common part A to part B ratios are 10:1 or 1:1 by weight. Although the reaction is initiated at room temperature, it can be accelerated using elevated temperatures.

Properties

Polymers exhibit a characteristic temperature called the glass transition temperature T_g, i.e. the temperature at which a polymer is converted between a glassy (= hard and brittle) and rubbery (= soft and flexible) state. The lower the glass transition temperature, the more the polymer can be cooled before it loses its flexibility and becomes glassy. The glass transition temperature of PDMS, $\sim -125\,^{\circ}C$, is reported to be very low compared to other common polymers. This implies that PDMS is an extremely flexible polymer, even liquid, at room temperature [39, 42].
The extreme flexibility of the backbone has several consequences. Although the backbone consists of polar silicon-oxygen bonds, polydimethylsiloxanes are extremely hydrophobic. This can be explained by a maximum number of methyl groups shielding the backbone, thereby reducing the surface energy and lowering the surface tension [41]. The shielding methyl groups also result in low intermolecular forces. This can be noticed in several ways, e.g. by the high permeability to gases, properties which do not change much with temperature or the liquid state even at high molecular weights.
As explained in the previous section, the polydimethylsiloxanes can be cross-linked to form silicone elastomers. The properties of the silicone elastomer are highly dependent on the structure of the polymer and the cross-linker. High and low cross-linking densities will result in hard and soft elastomers, respectively. Furthermore, fillers can be used to optimize the silicone elastomers in many different ways: reinforcement fillers (e.g. silica) can be added to improve mechanical properties such as shear, tensile strength and tear strength, while functional fillers such as thermally and electrically conductive fillers can be added to improve the respective properties.

Selection

The prime requirements for the silicone elastomer are:

- Non-toxicity / biocompatibility: to retain the possibility of biomedical applications.

- Ability to monitor optically: both for stretchable electronics and microfluidics, the ability to optically monitor processes through the silicone elastomer (e.g. by optical microscopy) is advantageous. The silicone elastomer is thus preferably transparent or translucent.
- Electrically insulating
- Low viscosity: the silicone elastomers are applied in three different manners in the experimental work, i.e. casting, injection molding and spin coating. A low viscosity is thus preferred.
- Sufficient working time: allow enough time for degassing and application.

Selection of an appropriate silicone elastomer based on these requirements (biocompatibility being the most stringent requirement) is in many cases not unique. Different silicone elastomers were considered: Sylgard® 184, Sylgard® 186 and Silastic® MDX4-4210 from Dow Corning, and MED-6010 and MED-6015 from NuSil. Although Sylgard® 184 and Sylgard® 186 are not classified as biocompatible, they were used for quick or initial tests because they are easy to work with. The three alternatively mentioned silicone elastomers are biocompatible, and differ mainly in viscosity. Depending on the method of application and desired layer thickness, an appropriate silicone elastomer is chosen.

Processing guidelines

Mixing and vacuum deaeration The different components which will cross-link to form the silicone elastomer are thoroughly mixed. The mixing ratio is specified in the product data sheet. Air which is entrapped during the mixing can be removed by exposing the PDMS to a vacuum in its liquid state for a time which depends on the viscosity. In this work, a vacuum of approximately -900 mbar was used. Release of the vacuum during the deaeration helps to break the bubbles that form.

Working time Cross-linking occurs as soon as the different components of the silicone elastomer are mixed. The rate of cross-linking determines the working time, i.e. the time that elapses from catalysis to the silicone mixture not longer being workable. The working time is dependent on the type of silicone and can range from a couple of minutes to several hours. Therefore, as a practical guideline throughout this dissertation, silicone mixtures are applied in their final form whenever they are free of air.

Curing Silicones can be cured at a wide range of temperatures ranging from room temperature to 150 °C. Typical curing times at room temperature range from 24 h to 72 h, and can be reduced to tens of minutes at elevated temperatures.

However, because of its high CTE, ranging from 300 ppm $^{\circ}C^{-1}$ to 400 ppm $^{\circ}C^{-1}$, curing (exposure) of silicone elastomers at (to) very high temperatures is generally avoided. This is especially the case when it is used for soft lithography (see Chapter 5).

Adhesion promoters Monomeric silicon chemicals are known as silanes, while silanes that contain at least one silicon-carbon bond are known as organosilanes. Organo-functional silanes on the other hand are organosilanes that carry two different reactive groups on their silicon atom so that they can react and couple with very different materials [43].
Frequently, adhesion promoters are required to enhance the adhesion of silicone elastomers to other substrate surfaces (e.g. silicones, plastics or metals). The primers are specially formulated organo-functional silanes supplied in a solvent. Its organo-functional component bonds into the silicone matrix while the hydrolyzable group bonds to the substrate. They generally have low surface tensions, ensuring good surface wetting.

Volatility It is known that lower molecular weight polydimethylsiloxanes can migrate out of the cured silicone elastomer matrix, resulting in contaminants [44]. To avoid outgassing e.g. in vacuum equipment or ovens, which could readily result in adhesion problems in other processes due to the low surface energy of polydimethylsiloxanes, silicone elastomers are solely processed in dedicated equipment. Processing steps such as the sputter deposition of metals on or reactive ion etching of silicone elastomers were thus not considered in this work.

2.5 Conclusions

The concept for the realization of conformable, stretchable electronics has been introduced. A pixelated architecture fixated on an elastomeric substrate is proposed: various non-stretchable islands are connected by stretchable electrical interconnections, which are able to deform with the elastomeric substrate without compromising the functionality. Meandering horseshoe shaped metallic conductors and thinning of dies are described in detail as these technologies form the basis of the packaging strategy. In addition, microfluidic technologies have been introduced: traditional and soft-lithographic techniques to pattern PDMS have been reviewed.
Several of the materials, such as the metallic conductors, the type of polyimide and the diverse silicone elastomers, which are used throughout the course of this PhD research have been discussed in detail. Thin-film gold was selected as metallic conductor based on its high conductivity, non-toxicity and ability to achieve fine-pitch metallization schemes. Based on the prime requirements for the polyimide, i.e. high-resolution patterning, non-toxicity, low stress and electrical in-

sulation, PI-2611 was selected. The silicone elastomer type, on the other hand, was not uniquely selected despite the stringent requirements. Depending on the method of application and desired layer thickness, the most appropriate silicone elastomer is chosen.

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3
Thin-film stretchable electrical interconnections

3.1 Introduction

To date, a variety of strategies towards the realization of stretchable electronic systems have been reported in literature; these are reviewed in Section 1.1.3. Focus is generally put on the development of stretchable electrical interconnections. These allow coping with relatively large mechanical strains without compromising their functionality, and connect various non-stretchable islands. It is clear that this is also the case for the realization of stretchable, conformable electronics presented in Section 2.2.

Two major trends for the realization of stretchable electrical interconnections are distinguished. One involves the use of primarily organic materials, e.g. intrinsically stretchable composite elastomer conductors, whereas the other trend focuses on the use of conventional high-performance inorganic electronic materials by devising ingenious structural designs to introduce stretchability. The former materials mainly comprise elastomers filled with electrically conductive particles, such as silver nanoparticles or carbon nanotubes. Their resistivity and other properties are however highly dependent on the filler concentration [1, 2]. Furthermore, the resistivity is typically quite large (easily three to four orders of magnitude higher than common metallic conductors), and a function of strain and environmental conditions (e.g. temperature) [3–5]. It is clear that such behavior is generally not desired for electrical interconnections. Therefore, in this disser-

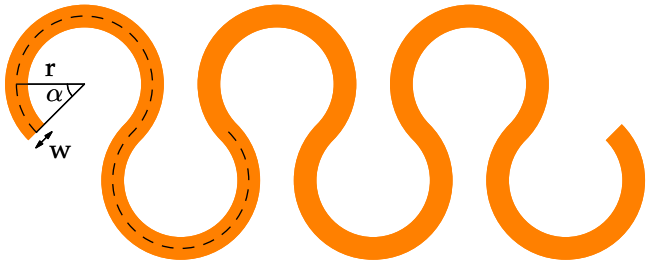


Figure 3.1: Stretchable electrical interconnections are realized by meandering horseshoe shaped metallic conductors.

tation, a strategy based on the latter trend is pursued. The interconnections are realized by meandering horseshoe shaped metallic conductors (Figure 3.1) that are able to function as two-dimensional springs when embedded in a silicone elastomer.
In the first section of this chapter, the fabrication process is described in detail. During technology development, special attention is paid to retain the possibility of biomedical applications, but also to improve the lifetime during cyclic mechanical loading. The process is demonstrated by fabricating test structures consisting of horseshoe shaped interconnections designed along straight parallel lines. The mechanical design parameters (angle α, radius r and width w, indicated in Figure 3.1) were fixed, but not optimized in terms of mechanical performance. The remainder of the chapter deals with the evaluation of the test structures.

3.2 Fabrication process

The fabrication process for the stretchable electrical interconnections is described in detail, and demonstrated by the realization of test structures. At this point, it is important to remark that several measures to delay the failure mechanisms described in Section 2.2.2, i.e. crack formation and crack propagation, were considered throughout the technology development.

- Fine-line metallization schemes were suggested to reduce the stress magnitudes in the horseshoe shaped metallic conductors. Therefore, thin-film metallization is featured to enable a fine interconnection pitch and conductor width by restricting underetch.

- Proper polyimide support is introduced for the metallic conductors to delay the crack propagation. By allowing freedom in design of the polyimide support, also the plastic strain in the metallic conductors can be reduced.

- Processing is done on a temporary carrier; transfer to an elastomeric substrate is performed in a final stage of the fabrication process. This implies a degree of freedom in the choice of the elastomeric substrate material, as its characteristics (properties, thickness, shape, etc.) do not affect the fabrication process up to the point of embedding.

3.2.1 Overview

A schematic representation of the fabrication process for the stretchable electrical interconnections is shown in Figure 3.2. Each step will be discussed in detail in the following, corresponding sections. The fabrication is started by cleaning a glass substrate (Figure 3.2(a)) and depositing a release stack (Figure 3.2(b)). Next, polyimide is spin coated (Figure 3.2(c)) and gold metallization is sputter deposited (Figure 3.2(d)). The metallization is patterned using photolithography and wet etching (Figure 3.2(e)), and covered by depositing another polyimide film (Figure 3.2(f)). A hard mask is then applied (Figure 3.2(g) and Figure 3.2(h)) and both supporting polyimide films are patterned in a single dry etch step to form polyimide covered meandering conductors (Figure 3.2(i) and Figure 3.2(j)). At a final stage of the fabrication process, the circuit is transferred to PDMS by a two-step embedding procedure (Figure 3.2(k) and Figure 3.2(l)).
To improve the clarity of this section, a unique name for each of the different layers of polyimide and PDMS is presented in Figure 3.3. This nomenclature will be used throughout the entire section.

3.2.2 Substrate

During fabrication, multiple layers of polyimide and photoresist are spin coated and aligned, various layers are thermally cured using temperatures varying from 120 °C up to 350 °C, metallization is sputter deposited, polyimide is dry etched, etc. It is quite clear that the quality and reproducibility of the diverse processing steps depends on the substrate used throughout the fabrication process.

Selection

White float glass from Präzisions Glas & Optik GmbH is chosen as substrate, and is available in different sizes and thicknesses. In this work, square glass substrates with a side length of either 2 inch (5.08 cm) or 4 inch (10.16 cm) were used, and had a thickness of 700 µm ± 50 µm. They are thermally stable during the high-temperature curing profile of polyimide PI-2611 (strain point: 490 °C ± 10 °C [6]) and have a limited CTE of 8.7 ppm $°C^{-1}$ [6], which closely matches that of the selected polyimide PI-2611 (3 ppm $°C^{-1}$).

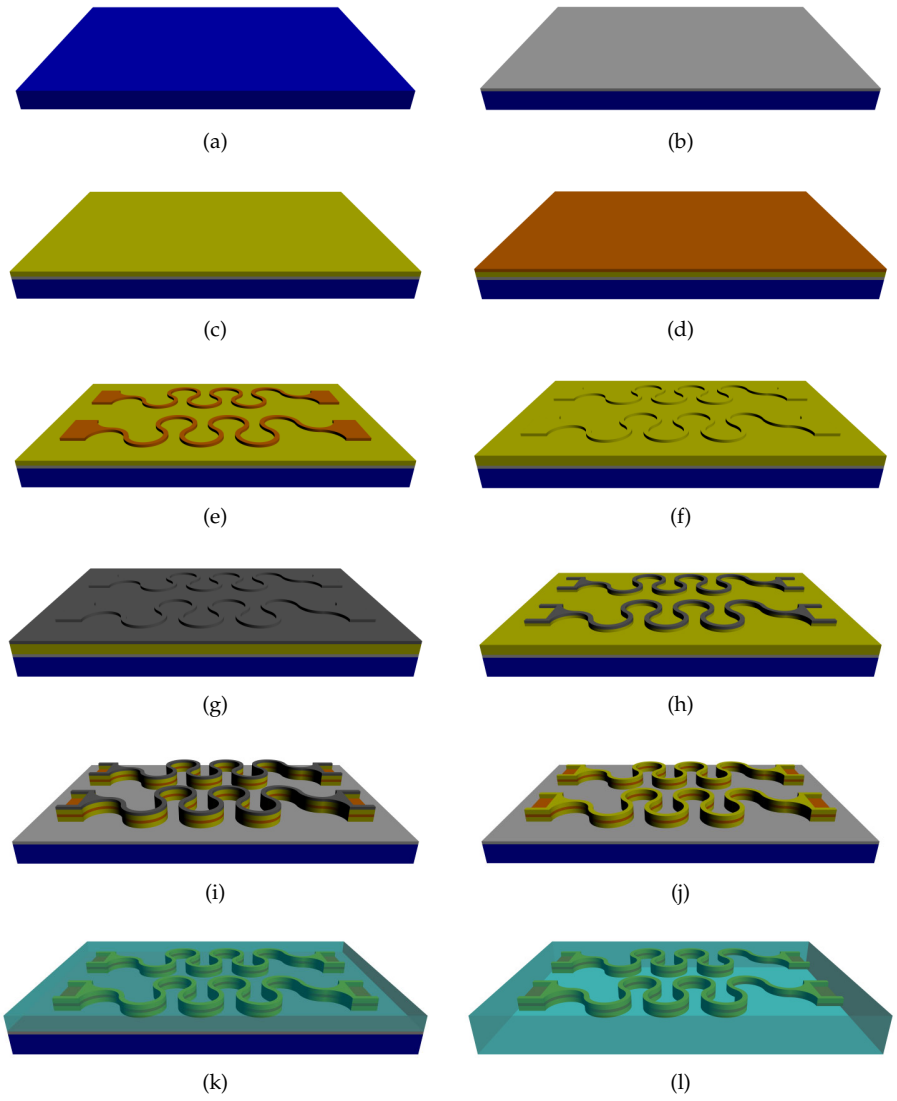


Figure 3.2: Fabrication process for stretchable electrical interconnections (not drawn to scale; a brief description is found in Section 3.2.1).

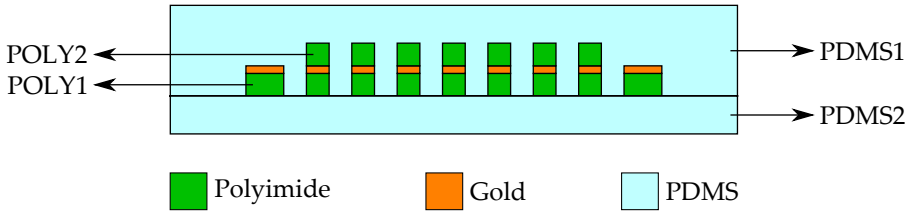


Figure 3.3: Stretchable electrical interconnections: nomenclature for the different layers of polyimide and PDMS (not drawn to scale).

Step #	Description	Parameters
(a)	Rinse in a beaker with detergent	1 night
	USA in a beaker with detergent	5 min
(b)	USA in a first beaker with DI	5 min
	USA in a second beaker with DI	5 min
	Rinse with DI pistol	
(c)	Rinse in a first beaker with IPA	2 min
	Rinse in a second beaker with IPA	2 min
(d)	USA in a first beaker with DI	5 min
	USA in a second beaker with DI	5 min
	Rinse with DI pistol	
(e)	Dry with nitrogen flush	
	Dry in a convection oven	30 min at 90 °C

Table 3.1: Cleaning procedure for the glass substrates.

Cleaning

Prior to processing, the glass substrates are thoroughly cleaned to remove organic residues. This was found necessary in order to prevent premature detachment of the release stack during wet processing. The cleaning procedure normally comprises a detergent (strongly diluted RBS T 105), isopropyl alcohol and deionized water soak sequence, and is summarized in Table 3.1.

3.2.3 Release layer stack

As illustrated in the schematic representation of the fabrication process (Figure 3.2), the transfer to PDMS is performed at a final stage of the fabrication process. This requires the complete stack displayed in Figure 3.2(j) to be separated from the glass substrate and has been proved quite challenging due to the diverse pro-

cessing conditions.

Selection criteria for the release procedure

Release procedures typically involve the deposition of sacrificial materials which are removed at a later stage. For this particular case, it is clear that the sacrificial material is present during the complete fabrication process. It should thus not be damaged during the subsequent processing steps, nor should its presence compromise the quality of the process. Therefore, before giving an overview of the possible release procedures, the major requirements imposed by the fabrication process are listed.

- The stack to be released (Figure 3.2(j)) is composed of several layers of PI-2611 which are cured using a high-temperature profile up to 350 °C. The high-temperature profile greatly limits the choice of sacrificial materials.
- The first layer of the stack is composed of PI-2611, which is supplied as a polyamic acid dissolved in an n-methyl-2-pyrrolidone (NMP) based solvent carrier. This is a powerful polar solvent which strongly dissolves organic materials as well as photoresists. Any sacrificial material in direct contact with liquid PI-2611 thus has to be compatible with NMP.
- The various wet processing steps including the etching of aluminium, gold and titanium tungsten, photoresist development, photoresist strip in acetone, etc. may not cause premature stack release. Hence, either the sacrificial material is compatible with or shielded from the wet chemicals.
- In addition, the release of the stack can be performed in an easy, not time-consuming way since large structures have to be released. Preferably, no harsh chemicals are used to avoid damaging the stack.

Overview of release procedures

Diverse sacrificial materials have already been demonstrated in literature ranging from materials removed by wet chemical etching, dry etching or dissolution in an appropriate solvent to thermally released temporary adhesives. Release procedures involving the former three are typically diffusion-limited [7, 8]. As a consequence, release of large structures or complete surfaces generally turns out to be time-consuming as large under-etch distances are encountered. Furthermore, the structures to be released are exposed to the etchant for a considerable amount of time which can result in device damage. One workaround consists in the integration of additional etch holes in the covering layers to speed up the removal of the sacrificial material [9]. However, the etch holes restrict the design freedom, need to be integrated in all covering layers and may decrease the performance of the structures to be released.

Anodic metal dissolution has been reported to be significantly faster than its diffusion-limited chemical etching variant [10]. In the cited work, a metal stack consisting of a base chrome and a top aluminium layer is deposited prior to the structures to be released. The aluminium layer functions as sacrificial material and is electrochemically removed in a sodium chloride solution when a positive potential is applied. The chrome layer maintains an electrically conductive path as the aluminium is removed, and is not dissolved. Although the release of microstructures composed of various materials such as SU-8, polyimide and platinum has already been illustrated, release is still time-consuming and highly dependent on stack buildup properties such as thickness and mechanical properties [10].
In contrast to the above-mentioned release procedures, thermally released temporary adhesives are typically area-independent and hence ideally suited to release large structures. The temporary adhesive is simply heated to a predefined temperature to cause detachment. An extra cleaning step may be required to remove adhesive residues. However, at the moment of process development, none was found to be compatible with the high-temperature curing profile of PI-2611.
Alternative release procedures for polyimide do not include the use of sacrificial materials. Laser release methodologies ablate a sub-micron layer of polyimide when the laser is incident on the substrate/polyimide interface through a transparent substrate. The efficacy is determined by three closely related factors: the laser radiation wavelength, the transparency of the substrate at the wavelength and the ease of ablation of the selected polyimide. Release of polyimides has already been illustrated with XeCl [11] and ArF [12] excimer lasers, corresponding with wavelengths of 308 nm and 193 nm respectively. However, from transmission measurements of common substrate materials, it was apparent that cheaper substrates such as glass and pyrex are not sufficiently transparent at these wavelengths. Laser release methodologies thus do not only implicate access to a suitable laser, but also require the use of more expensive substrates such as polished quartz substrates.
Also the bad adhesion of polyimide to certain substrates has been exploited to perform release. Selective application of an adhesion promoter at the perimeter of silicon or glass substrates results in polyimide films which are nicely adhered at the edges, while marginal adhesion elsewhere is obtained [13]. Parts of the polyimide film can thus be released by selective pattern definition.

Customized release layer stack

Despite the variety of release procedures, none was found fully complying with the above-mentioned fabrication process. Therefore, a customized release procedure was developed. Potassium chloride (KCl) is chosen as a base material since it is chemically inert, has a melting point of 773 °C (according to its MSDS [14]) and can easily be released at a later stage by dissolution in deionized water.

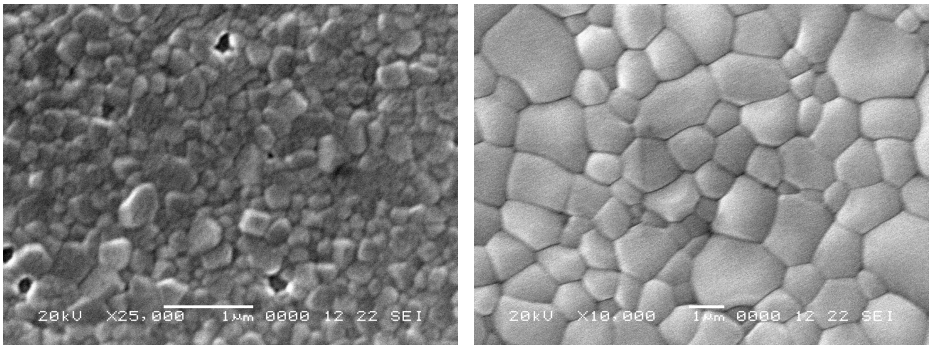
Figure 3.4: Aluminium foil is wrapped over the substrate edges and serves as a shadow mask for the evaporation of potassium chloride.

A uniform film is deposited on a clean glass substrate by thermal evaporation (resistive heating) in a Leybold-Heraeus Univex 450 system. To this end, a refractory molybdenum crucible is filled with approximately 3 g of potassium chloride (99.999 Suprapur®, Merck Chemicals), and current is applied to the crucible to heat the material. The current is set so that a fixed deposition rate of $5\,\text{Å}\,\text{s}^{-1}$ is achieved, resulting in a chamber pressure of 4×10^{-6} mbar. This deposition rate was chosen out of practical considerations in order to limit the time required to evaporate films with anticipated thicknesses of several hundred nanometers.

To prevent premature stack release during the subsequent wet processing steps, a shadow mask is used to prevent potassium chloride from being deposited at the edges of the substrate. To this end, aluminium foil is wrapped over the substrate edges before deposition as depicted in Figure 3.4, and serves as a shadow mask since it is removed after the deposition.

To determine the right film thickness, different thicknesses of deposited potassium chloride ranging from 50 nm to 400 nm were investigated by means of scanning electron microscopy. Depending on the deposited thickness, a different surface topography of the potassium chloride layer is obtained. The SEM image of a 100 nm thick layer is shown in Figure 3.5(a), clearly indicating the presence of pinholes. These pinholes result in local adhesion of the subsequently deposited layer to the glass substrate and will later on hamper a successful release. Figure 3.5(b) shows the surface topography of a 400 nm thick layer where no pinholes are detected, and which will eventually be used for a successful release.

Next, a 5.5 µm thick sacrificial layer of PI-2611 is spin coated on top of the potassium chloride film and ensures effective shielding against moisture penetration after curing. This continuous polyimide film was found indispensable to prevent premature stack release. Furthermore, it was chosen to be part of a sacrificial stack (i.e. it will be removed at a later stage of the fabrication process) because



(a) Thickness: 100 nm; pinholes are clearly present.

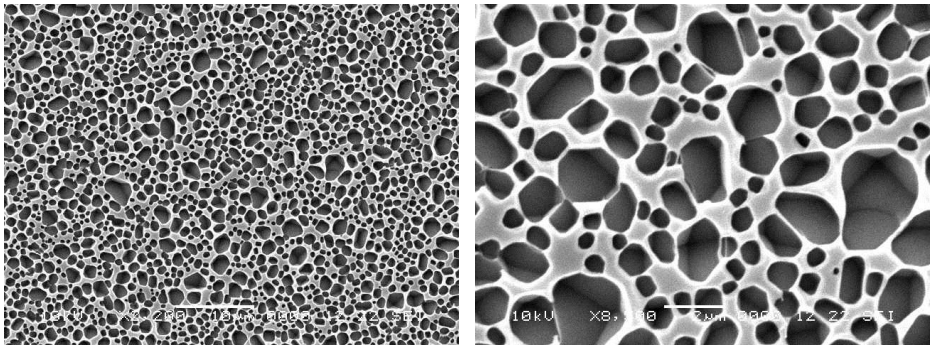
(b) Thickness: 400 nm; no pinholes are detected.

Figure 3.5: Surface topography of evaporated potassium chloride with different thicknesses.

the polyimide film spin coated and cured directly on top of the potassium chloride was found to suffer from increased brittleness. This is explained by an increased porosity of the polyimide at the KCl/PI-2611 interface, as demonstrated by the SEM images in Figure 3.6. These display the backside of a released PI-2611 film which was spin coated and cured directly on top of a 400 nm thick layer of potassium chloride.

As the sacrificial polyimide layer should not be attacked during the structuring of the polyimide layers supporting the stretchable interconnections (Figure 3.2(j)), an additional 50 nm titanium tungsten adhesion layer and 1 µm thick aluminium film are sputter deposited to serve as an etch stop between the structural and sacrificial polyimide films. Sputter deposition of these metal films directly on top of the potassium chloride was found to be ineffective as the shielding layer during the wet processing steps. Both a 1 µm thick film of copper and aluminium on top of the 50 nm titanium tungsten adhesion layer immediately caused detachment when immersed in deionized water.

The release stack is thus composed of three layers: a 400 nm thick potassium chloride layer which is evaporated using a shadow mask, a 5.5 µm thick film of PI-2611 and a 1 µm thick aluminium film, preceded by a 50 nm thick titanium tungsten adhesion layer. This is schematically represented in Figure 3.7. Since the release stack consists of 3 layers, release and stripping are performed in several phases. First, an incision is made according to the desired outline for the circuit through the complete release stack. Next, the substrate is placed in a beaker with deionized water to dissolve the potassium chloride. The stack is then easily separated from its rigid carrier (Figure 3.14(a)), followed by backside etching of the



(a) Scale bar: 10 µm. (b) Scale bar: 2 µm.

Figure 3.6: Increased porosity of the polyimide at the KCl/PI-2611 interface.

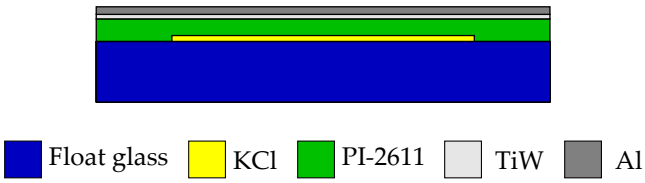


Figure 3.7: Cross-sectional view of the release layer stack (not drawn to scale).

shielding polyimide and titanium tungsten/aluminium films by dry etching and wet etching, respectively, according to the procedures described in Section 3.2.6. In Figure 3.8, test patterns are shown which are transferred to Silastic® MDX4-4210 using the presented release procedure. Horseshoe shaped interconnections with a track width down to 20 µm were successfully transferred.

3.2.4 Application of PI-2611

During fabrication of the stretchable electrical interconnections, two layers of PI-2611 are deposited: a base layer (POLY1) on which the metallization is deposited (Figure 3.2(c)) and a second layer (POLY2) to cover the metallization (Figure 3.2(f)). The polyimide layers are applied by spin coating; identical parameters were chosen for each layer. Spin coating is started by manually dispensing approximately 1 ml of PI-2611 in the center, close to the substrate. In the product data sheet [15], it is suggested that the acceleration to the final speed is as slow as possible to allow the coating to flow across the substrate. Therefore, an intermediate spin speed of 500 rpm is used to gradually cover the substrate before

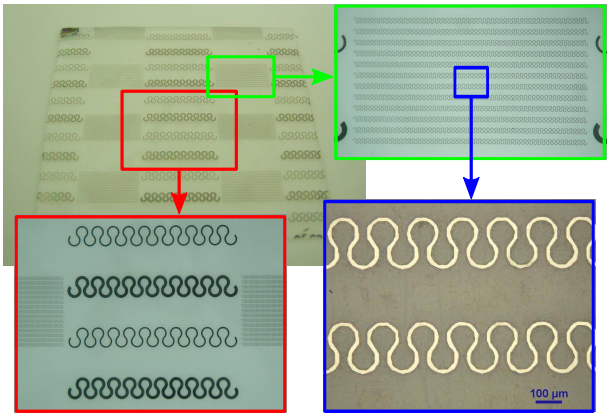


Figure 3.8: Test patterns transferred to Silastic® MDX4-4210; the track width in the pictures on the right is 20 µm (scale bar: 100 µm).

Step #	Description	Parameters
(a)	Apply shadow mask	Al foil
	Evaporate KCl	Thickness: 400 nm,
	(Leybold Heraeus Univex 450)	Chamber pressure: 4×10^{-6} mbar,
		Deposition rate: 5 Å s^{-1}
	Remove shadow mask	
(b)	Apply PI-2611	See Table 3.3
(c)	Sputter deposit TiW	Thickness: 20 nm,
	(Leybold Z550)	DC power: 1200 W,
		Chamber pressure: 1×10^{-2} mbar
	Sputter deposit Al	Thickness: 1 µm,
	(Leybold Z550)	DC power: 2000 W,
		Chamber pressure: 2×10^{-3} mbar

Table 3.2: Process parameters for the application of the customized release layer stack.

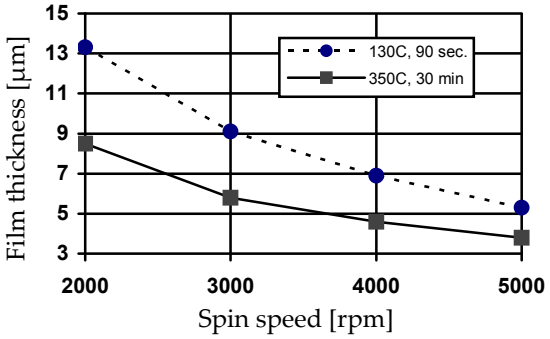


Figure 3.9: Spin speed curve for PI-2611, coated for 30 s at the indicated speed. The dashed and continuous line indicate the film thickness after soft bake and full cure respectively [15].

continuing to the final spin speed. The final spin speed and spin time determine the thickness of the coating, and can be deducted from the spin speed curve in Figure 3.9. In this work, a coating thickness of 5.5 µm after final cure was chosen, corresponding to a final spin speed of 3000 rpm.

After spin coating, the polyimide is cured, converting the polyamic acid precursor into a fully aromatic, insoluble polyimide film and driving off the NMP solvent carrier. The curing is performed using a temperature profile with a gradual ramping up to 350 °C in an inert nitrogen atmosphere. Both a vacuum oven and nitrogen flushed oven can be successfully used for this purpose. After loading, the latter is excessively flushed with nitrogen to make sure that an inert atmosphere is obtained before and during temperature ramping. Also during cure in the vacuum oven, nitrogen is bled into the chamber.

In the following subsections, the different layers of PI-2611 will be shortly discussed as different pretreatments of the underlying layer are required, but also different criteria are used to evaluate the quality of the deposited film.

POLY1

The first layer of PI-2611 is spin coated on top of the 1 µm thick aluminium film which is part of the release layer stack (Figure 3.7). Although it is suggested to use an aminosilane based adhesion promoter such as VM-651 or VM-652 (HD Microsystems^{TM}) to enhance adhesion on materials like silicon, ceramic and metals, it was found unnecessary as sufficient adhesion is readily obtained.

Step #	Description	Parameters
(a)	Manual, static dispense	Approximately 1 ml
(b)	Spin coat	Start at 500 rpm, Hold 5 s at 500 rpm, Ramp to 3000 rpm at 250 rpm s^{-1}, Hold 30 s at 3000 rpm
(c)	Bake	Hotplate, 10 min at 200 °C
(d)	Final cure (inert atmosphere)	Ramp to 200 °C at 4 °C min^{-1}, Hold 30 min at 200 °C, Ramp to 350 °C at 2.5 °C min^{-1}, Hold 60 min at 350 °C, Gradually cool to RT

Table 3.3: Process parameters for the application of PI-2611.

POLY2

The second coating of polyimide is used to cover the gold metallization. To improve the adhesion to POLY1, the surface of POLY1 is slightly roughened by exposing it briefly for 1 min to an oxygen (O_2) plasma prior to the application of POLY2. A System VII Batchtop RIE (Plasma-Therm) was used for this purpose with following parameters: RF power 150 W, O_2 flow rate 25 sccm and chamber pressure 150 mTorr.

3.2.5 Metallization

A uniform gold film is sputter deposited on POLY1 (Figure 3.2(d)), and subsequently patterned via photolithography and wet etching (Figure 3.2(e)).

Sputter deposition

The metallization is deposited by DC magnetron sputtering in an Alcatel SCM600 system. A 200 nm thick gold layer and a 50 nm thick titanium tungsten adhesion enhancement layer are deposited in the same vacuum cycle. The sputter deposition of these metals is an established process at the CMST research group and has been executed using the standard parameters without any modifications.
Sputter deposition is preferred over evaporation because of its better adhesion to the substrate. The adhesion to the polyimide was found to be poor without any pretreatments, despite the use of a titanium tungsten adhesion enhancement layer. To improve the adhesion, the polyimide surface is slightly roughened using a brief exposure to an oxygen (O_2) plasma as described in Section 3.2.4. Actually, this step has to be performed just once: by roughening the surface of POLY1 prior

Step #	Description	Parameters
(a)	Sputter deposit TiW	Thickness: 50 nm,
	(Alcatel SCM600)	DC power: 1200 W
		Chamber pressure: 1×10^{-2} mbar
	Sputter deposit Au	Thickness: 200 nm,
	(Alcatel SCM600)	DC power: 1000 W,
		Chamber pressure: 1×10^{-2} mbar
(b)	Spin coat S1818	60 s at 4000 rpm
	Soft bake	Hotplate, 2 min at 90 °C
	UV exposure	7.5 s at 10 mW cm^{-2}
	Development	50 % Microposit^{TM} developer, 35 s
	Hard bake	Convection oven, 30 min at 120 °C
(c)	Wet etch Au	Au etchant (see text), on sight
	DI rinse	2 min
	Wet etch TiW	30 % H_2O_2, 25 s at 55 °C
		30 % H_2O_2, 10 s at RT
	DI rinse	2 min

Table 3.4: Process parameters for the metallization.

to the sputter deposition of the metallization, also the adhesion of the second polyimide film POLY2 is improved as the surface of POLY1 sustains its roughness after pattern definition of the metallization.

Pattern definition

The metallization is patterned via photolithography and wet etching. To this end, positive photoresist S1818 is used as a masking layer to wet etch both metal films. A 1.8 µm thick S1818 coating is spin coated at 4000 rpm for 60 s, soft baked on a hotplate for 2 min at 90 °C, UV exposed for 7.5 s at 10 mW cm^{-2}, developed for 35 s in 50 % Microposit^{TM} developer and hard baked for 30 min in a convection oven at 120 °C.

After applying the photoresist, the metallization is wet etched. A solution of iodine (I_2) and potassium iodide (KI) with a mixing ratio of KI : I_2 : DI = 4 g : 1 g : 73 ml is used to pattern the gold. The etching is performed at room temperature and stopped on sight because the etch rate is highly dependent on the mechanical agitation. The underlying titanium tungsten layer is etched in a 30 % H_2O_2 solution at 55 °C for 25 s, followed by a 10 s rinse in a 30 % H_2O_2 solution at room temperature and rinse in deionized water.

3.2.6 Structuring of PI-2611

After covering the patterned metallization with another layer of PI-2611 (POLY2; Figure 3.2(f)), both POLY1 and POLY2 are structured to achieve polyimide supported meandering conductors (Figure 3.2(j)). This is done by dry etching, as patterning PI-2611 films using traditional wet etch techniques is difficult due to the molecular structure and inherent film density.

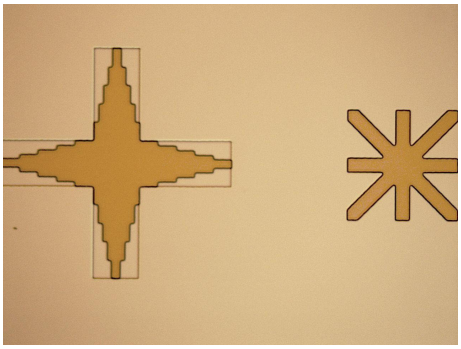
Masking layer

An etch mask is required to pattern the PI-2611 films by dry etching. To this end, a 20 nm thick titanium tungsten adhesion enhancement layer and a 200 nm thick aluminium film are sputter deposited in the same vacuum cycle. Aluminium is the preferred hard mask since it is inert for the oxygen (O_2) and trifluoromethane (CHF_3) chemistry used to etch PI-2611.

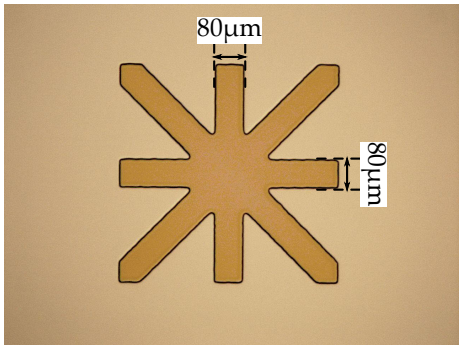
Both metal films are patterned via photolithography and wet etching. To this end, a 1.8 µm thick S1818 coating is spin coated at 4000 rpm for 60 s, soft baked on a hotplate for 2 min at 90 °C, UV exposed for 7.5 s at 10 mW cm^{-2}, developed for 35 s in 50 % Microposit^{TM} developer and hard baked for 30 min in a convection oven at 120 °C. Note that the aluminium mask has to be aligned relative to the gold patterns. Height variations in the covering polyimide film POLY2 caused by the underlying gold patterns, as is clearly illustrated in Figure 3.10(a) and Figure 3.10(c), facilitate the aligning and exclude exposing the alignment marks using additional processing steps.

After application of the photoresist, the hard mask is wet etched. A solution of acetic acid (CH_3COOH, > 99 %), nitric acid (HNO_3, > 65 %) and phosphoric acid (H_3PO_4, > 89 %) with a mixing ratio of CH_3COOH : HNO_3 : H_3PO_4 : DI = 4 : 1 : 4 : 1 is used to pattern the aluminium film. The etching is performed at room temperature, without mechanical agitation. The etch rate is approximately 20 nm min^{-1}. Substrates are thoroughly rinsed in deionized water after etching to remove any residual acid. The underlying titanium tungsten layer is etched in a 30 % H_2O_2 solution at 55 °C for 15 s, followed by a 10 s rinse in a 30 % H_2O_2 solution at room temperature and rinse in deionized water. The photoresist is finally stripped using an acetone, acetone / isopropyl alcohol and deionized water soak sequence.

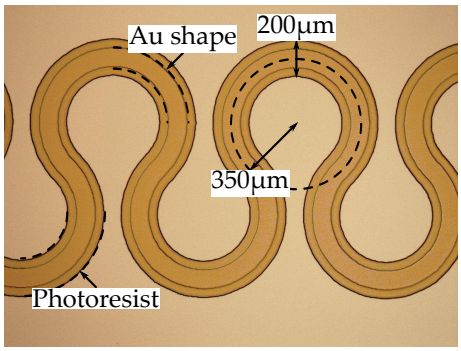
After dry etching, the hard mask is completely removed using an identical wet etch procedure. Both the hard mask and the aluminium film which is part of the release stack are exposed to the etchants. Because the latter has a thickness of 1 µm, the 200 nm thick hard mask can be removed without completely sacrificing the latter. Remember that the aluminium film which is part of the release stack is required to avoid contamination of the etch tool; refer to the paragraph on volatility in Section 2.4.3.



(a) Well-aligned alignment marks.



(b) Dimensions of an alignment mark.



(c) Well-aligned horseshoe shapes.

Figure 3.10: Aligning of the photoresist used to pattern the hard mask, relative to the gold patterns.

Parameter	Symbol	Level 1	Level 2
O_2:CHF_3 flow rates [sccm]	A	15:5	25:5
RF power [W]	B	100	200
Chamber pressure [mTorr]	C	75	150

Table 3.5: The two levels and corresponding values of the dry etching parameters.

Dry etching

Both supporting bottom and top polyimide films (POLY1 and POLY2, respectively) are subsequently patterned by dry etching. Dry etching conditions of polyimide typically depend on the etch tool and on processing details such as deposited film thickness and curing profile. Therefore, an optimization of the different dry etching parameters is performed based on a design of experiments (DOE). Running through all of the possible etch processes, as is the case with a full factorial experiment, requires a quantity of experiments which increases according to a power law with the number of process parameters. Such a basic DOE is generally both time consuming and expensive to implement.
The Taguchi method designs the experiments based on orthogonal arrays and allows for the study of a large parameter space with a limited number of experiments. It is used to predict the optimal combination of process parameters. Finally, a confirmation experiment is conducted to verify this prediction.

Optimization Three parameters are selected for optimization: RF power, chamber pressure and O_2:CHF_3 flow rates, with the constraint that the CHF_3 flow rate is kept constant at 5 sccm. A two-level orthogonal array is constructed to discover trends in the dry etching. The parameters values are based on values and ranges mentioned in the PI-2611 product data sheet [15]; these are listed in Table 3.5. Evaluation is done with respect to the etch rate and the etch uniformity over a surface area of approximately 5 cm by 5 cm.
Uniform PI-2611 films with a thickness of 5.5 µm were prepared by spin coating on clean glass substrates. A 20 nm thick titanium tungsten adhesion enhancement layer and 200 nm thick aluminium film were sputter deposited and patterned by photolithography and wet etching. The design used for this purpose is displayed in Figure 3.11. After the photoresist strip, dry etching of the PI-2611 films was conducted during 5 min using a System VII Batchtop RIE (Plasma-Therm). Finally, the aluminium hard mask was wet etched. Each processing step was performed in accordance with the corresponding sections in this chapter.
The etch depth was measured using an optical profiler WYKO NT3300 (Veeco). This was done at five well-distributed spots along the outline of a cross, one spot

(a) Complete mask design. (b) Zoomed view of the indicated part.

Figure 3.11: Mask design which is used to optimize the parameters for dry etching PI-2611.

at the centre of the substrate and four spots at approximately 5 mm from each of the substrate edges, and an average is calculated. The etch uniformity is quantified by calculating the RMS value related to these etch depths:

$$\text{Etch uniformity} = \sqrt{(d_2 - d_1)^2 + (d_3 - d_1)^2 + (d_4 - d_1)^2 + (d_5 - d_1)^2} \quad (3.1)$$

with d_1 and d_x (x = 2..5) the etch depths at the centre and at the edges of the substrate, respectively. A smaller RMS value implies a better etch uniformity. Both values are mentioned in Table 3.6 for the performed experiments. Figure 3.12 shows the trend lines for each parameter with respect to the etch depth and etch uniformity, i.e. the evolution of the evaluated quantity when the respective parameters are altered. It is noticed that the RF power is the most important parameter (largest slope) for both the etch depth and the etch uniformity, followed by the chamber pressure and the O_2:CHF_3 flow rate ratio (smallest slope). Increasing any of the parameters results not only in an increased etch rate, but also in a decreased etch uniformity. Hence, a trade-off analysis was made keeping in mind the significance of the different parameters. Levels 1.5, 2 and 1 are selected, corresponding to an RF power of 150 W, a chamber pressure of 150 mTorr and O_2:CHF_3 flow rates of 15 sccm:5 sccm, respectively. The analysis was also used to predict an average etch depth of 1.53 µm and etch uniformity of 8.59 nm. Experimentally, these were determined as 1.65 µm and 6.57 nm, respectively, closely corresponding to the predicted values.

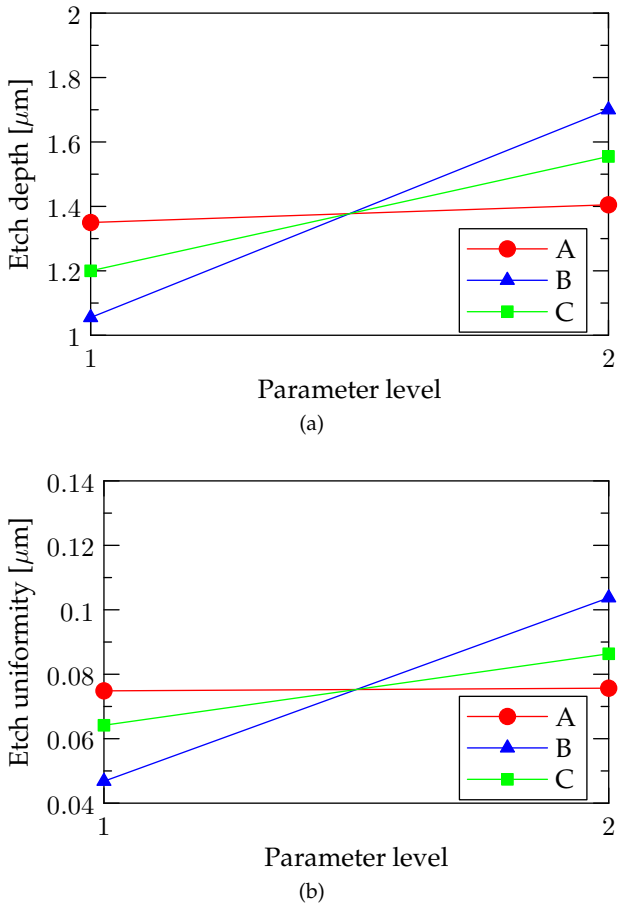


Figure 3.12: Trend lines for the dry etching parameters with respect to (a) the etch depth and (b) the etch uniformity.

	Parameter level			Response	
Experiment No.	A	B	C	Etch depth [µm]	Etch uniformity [nm]
1	1	1	1	0.87	4.90
2	1	2	2	1.92	12.2
3	2	2	1	1.57	13.4
4	2	1	2	1.29	8.90

Table 3.6: Experiments performed based on an L_4 (2^3) orthogonal array; dry etching of the PI-2611 films was performed for 5 min.

Structuring of PI-2611 to form the meandering conductor support The optimized dry etching parameters are used to etch both supporting bottom and top polyimide films, which have a total thickness of 11 µm. With an etch rate of 0.33 µm min^{-1}, the etch time is initially estimated to be approximately 33.3 min. However, it has to be kept in mind that the surface area to be etched also affects the etch rate. For the design displayed in Figure 3.17, the etch time was found to be 45 min.
It was also verified that the gold film, like the aluminium film, effectively serves as a masking layer for the dry etching, making it possible to provide contact pads to the gold conductors by etching the top polyimide film POLY2 (as schematically illustrated in Figure 3.2(j)).

3.2.7 Placement of components

Conventional off-the-shelf components (e.g. SMD) can be mounted on the exposed gold metallization. This is done by means of anisotropic or isotropic conductive adhesives as it is found impossible to perform regular soldering without damaging the 200 nm thick gold film because it dissolves too rapidly into the solder. Figure 3.13 displays Molex ZIF (zero insertion force) sockets which are mounted on exposed gold pads by means of an isotropic conductive adhesive CE 3104 (Emerson & Cuming). The ICA is cured in ambient atmosphere in a convection oven at 120 °C for 10 min.

3.2.8 Encapsulation in PDMS

Encapsulation in PDMS can be done either by spin coating or liquid injection molding, both in two phases to provide full encapsulation. The former method is chosen when thin, uniform films of PDMS are desired, while for the latter method the substrate is clamped in between two machined PMMA molds, offering the

Step #	Description	Parameters
(a)	Sputter deposit TiW	Thickness: 20 nm,
	(Leybold Z550)	DC power: 1200 W,
		Chamber pressure: 1×10^{-2} mbar
	Sputter deposit Al	Thickness: 200 nm,
	(Leybold Z550)	DC power: 2000 W,
		Chamber pressure: 2×10^{-3} mbar
(b)	Spin coat S1818	60 s at 4000 rpm
	Soft bake	Hotplate, 2 min at 90 °C
	UV exposure	7.5 s at 10 mW cm^{-2}
	Development	50 % Microposit^{TM} developer, 35 s
	Hard bake	Convection oven, 30 min at 120 °C
(c)	Wet etch Al	Al etchant (see text), 10 min
	DI rinse	2 min
	Wet etch TiW	30 % H_2O_2, 15 s at 55 °C
		30 % H_2O_2, 10 s at RT
	DI rinse	2 min
(d)	Strip S1818	Acetone, 2 min
	IPA rinse	2 min
	DI rinse	2 min
(e)	Dry etch PI-2611	45 min (see text)
	(System VII Batchtop RIE)	RF power: 150 W,
		Chamber pressure: 150 mTorr,
		O_2 flow rate: 15 sccm,
		CHF_3 flow rate: 5 sccm
(f)	Wet etch Al	Al etchant (see text), 10 min
	DI rinse	2 min
	Wet etch TiW	30 % H_2O_2, 90 s at 55 °C
		30 % H_2O_2, 10 s at RT
	DI rinse	2 min

Table 3.7: Process parameters for the structuring of PI-2611 to form the meandering conductor support.

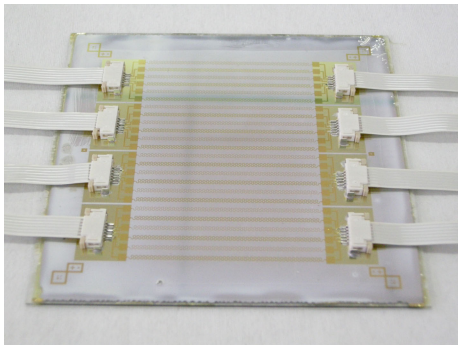


Figure 3.13: Molex ZIF sockets are mounted on exposed gold pads.

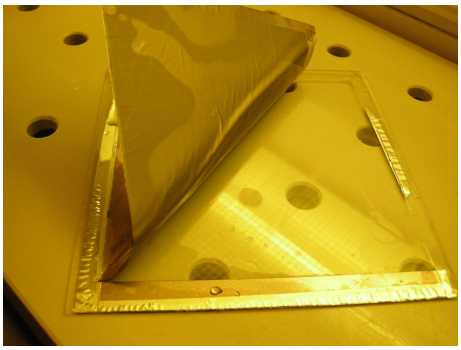
possibility of performing non-uniform 3-D encapsulation. Both methods have been used to encapsulate the test structures discussed in Section 3.3, illustrating the generic character of the technology with respect to the encapsulation procedure.

Two types of PDMS are used, Sylgard® 186 for liquid injection molding and Silastic® MDX4-4210 for spin coating. Prior to application of the first (but also the second) layer of PDMS, 1200 OS Primer is applied to the substrate for improved adhesion of the PDMS to the polyimide structures. To this end, the substrate surface is cleaned using a wipe with IPA. Next, a thin film (!) of the primer is applied using a clean wipe. As the primer is usually activated by atmospheric moisture, it is allowed to air dry for 15 min before applying the PDMS. If a white chalky residue is noticed, the residue is removed by means of a clean wipe.

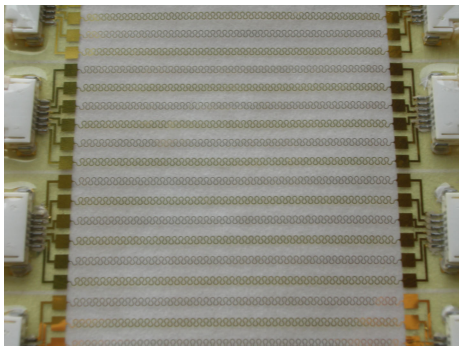
After applying the first layer of PDMS, it is cured for 4 h in ambient atmosphere in a convection oven at 50 °C (Figure 3.2(g)). The stack is then released from the rigid carrier, as illustrated in Figure 3.14(a), and the sacrificial layers are removed according to the procedure described in Section 3.2.3 (Figure 3.14(b)). Subsequently, the encapsulation procedure is repeated at the bottom side of the released membrane. Encapsulated test structures are shown in Figure 3.15(a) and Figure 3.15(b); the PDMS thickness is 2.5 mm and 1.2 mm, respectively.

3.3 Evaluation

To illustrate the capabilities of the presented fabrication technology, test structures consisting of horseshoe shaped interconnections designed along straight parallel lines were fabricated. These were used as a means to evaluate the (mechanical and electrical) performance of the stretchable electrical interconnections. The design and electrical performance are discussed in Section 3.3.1 and Section

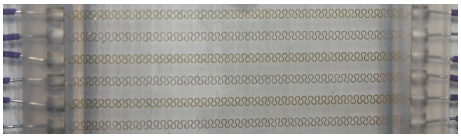


(a) Separation from the rigid carrier.

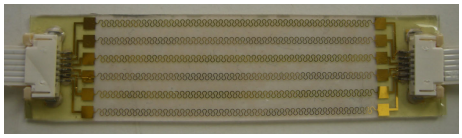


(b) The sacrificial layers are removed.

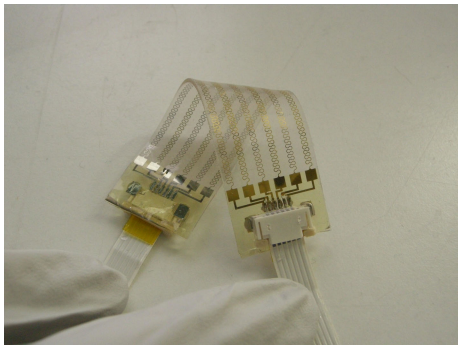
Figure 3.14: Stack with partially encapsulated horseshoe shaped interconnections is separated from its rigid carrier, and the sacrificial layers are removed.



(a) By liquid injection molding.

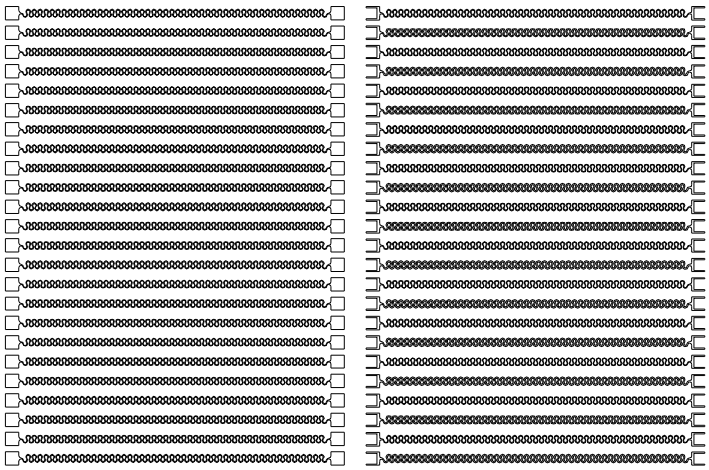


(b) By spin coating.



(c) Highly conformable test structures.

Figure 3.15: Test structures consisting of horseshoe shaped interconnections, fully encapsulated in PDMS.



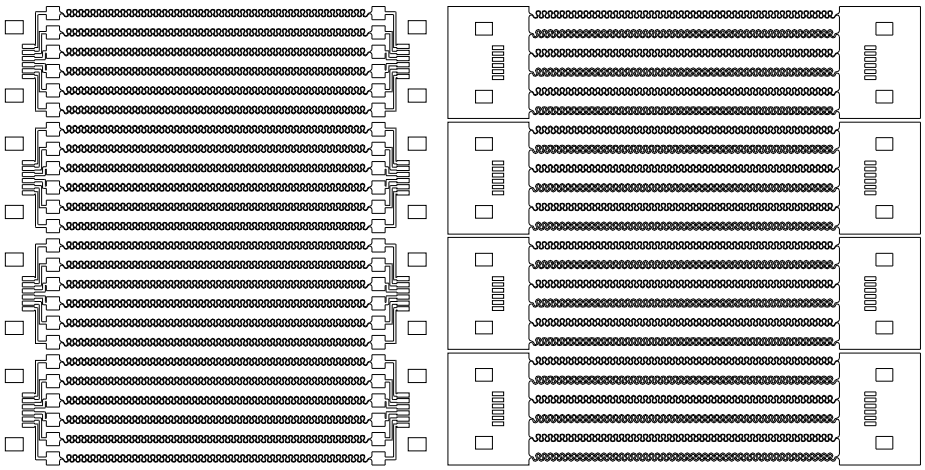
(a) Metallization. (b) Polyimide.

Figure 3.16: Mask design of the stretchable electrical interconnection test structures - version 1.

3.3.2, respectively. For the mechanical performance (Section 3.3.3), a distinction is made between one-time uniaxial stretching, performed on the test structures embedded by spin coating, and cyclic mechanical loading, performed on the test structures embedded by liquid injection molding.

3.3.1 Design of the test structures

Two versions of the test structures were fabricated; their mask design is displayed in Figure 3.16 and Figure 3.17. One version solely consists of stretchable electrical interconnections, electrically connected by metallic wires and encapsulated in PDMS by liquid injection molding. In the other version, off-the-shelf ZIF sockets were mounted on separated polyimide islands which are connected by stretchable electrical wiring and encapsulated in PDMS by spin coating.
The design of the stretchable interconnections is identical in both designs; solely the electrical connection towards the gold pads differs. The meandering horseshoe shaped interconnections have an unstretched point-to-point length (Figure 3.18) of 51.6 mm, and the mechanical design parameters indicated in Figure 3.1 were fixed at $\alpha = 45°$, r = 350 µm and w = 100 µm. These parameters were not optimized in terms of electrical or mechanical performance, but are well suited as a general indication [16, 17]. Furthermore, the line-to-line pitch, defined as the distance between corresponding points on adjacent tracks (Figure 3.18), was de-



(a) Metallization. (b) Polyimide.

Figure 3.17: Mask design of the stretchable electrical interconnection test structures - version 2.

signed to be 3.2 mm in order to minimize the effect of the interconnection pitch on the mechanical behavior of the stretchable interconnections [18].
As the integration of polyimide support for the meandering gold conductors is a key feature of the presented technology, two different widths for the polyimide support were included in the mask design of the test structures to illustrate its effect on the mechanical performance. Polyimide support widths of 100 µm, which is the same width as the gold conductor, and 200 µm, which is 100 µm wider than the gold conductor, were alternately included in the design. A zoomed view of the fabricated interconnections can be seen in Figure 3.19.

3.3.2 Electrical performance

Due to the tortuosity of the metallic conductors, the path length of the stretchable interconnections is clearly larger than the point-to-point length. The electrical resistance of the stretchable interconnections will thus clearly exceed the electrical resistance of conventional straight tracks. This has to be taken into account during the design of a stretchable electronic circuit.
Consider the design displayed in Figure 3.16; as mentioned in Section 3.3.1, the design of the stretchable interconnections running in between the test pads is identical to those of the design displayed in Figure 3.17. Although their point-to-point length is ~51.6 mm, the tortuous metallic conductors have a path length

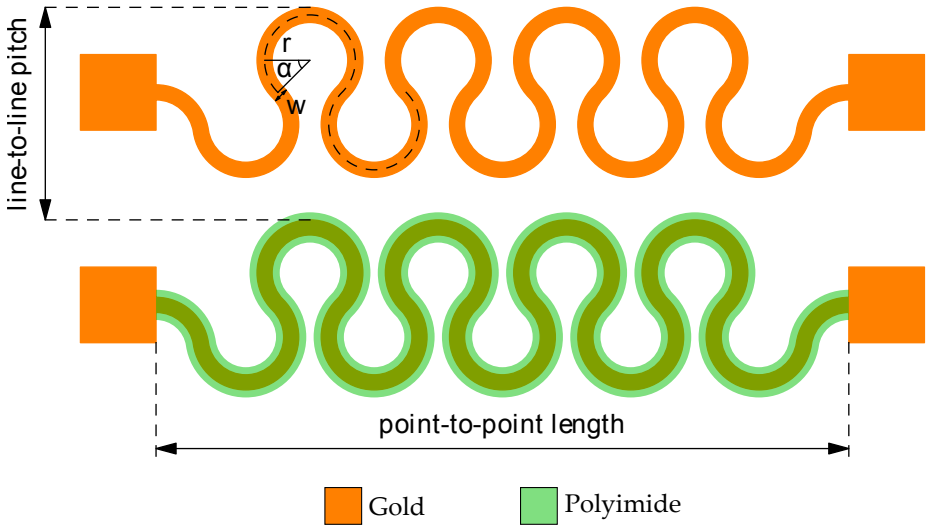
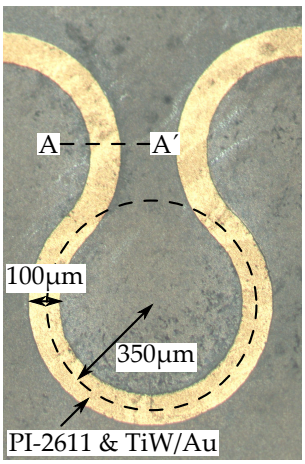


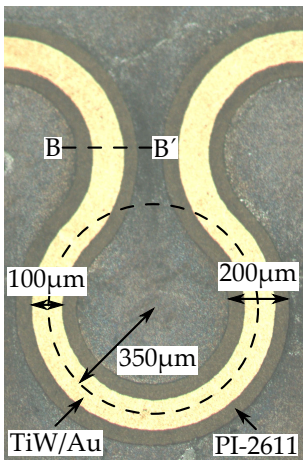
Figure 3.18: Schematic representation of the point-to-point length and line-to-line pitch for the horseshoe shaped interconnections.

of ~167.6 mm. Assume the resistivity of bulk gold ρ_{Au} at room temperature to be $2.44 \times 10^{-8}\,\Omega\,\mathrm{m}$, a common value found in literature [19]. The electrical resistance of these meandering horseshoe shaped interconnections is estimated to be ~204 Ω, whereas the electrical resistance of the corresponding straight track is ~3.25 times smaller.

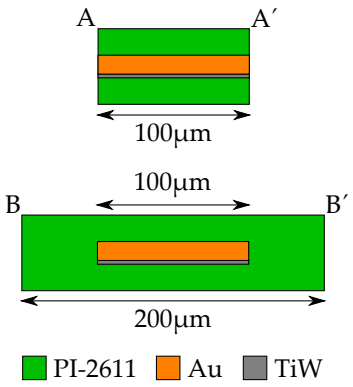
Measurements performed on substrates with the design displayed in Figure 3.17 showed electrical resistances ranging from 173 Ω at one side of the substrate, to 245 Ω at the opposite side. The deviation of the measured electrical resistance compared to the calculated value is explained by (a) the known difference in resistivity of bulk metal and sputtered thin-film metals, (b) the thickness of the gold film which deviates from the target thickness and (c) the additional electrical resistance of the straight tracks towards the ZIF sockets. The large range of values, on the other hand, is attributed to the linear thickness variation of the sputtered gold film over the length of the substrate. This phenomenon is inherent to the sputtering process at the CMST research group, and is a direct cause of the relatively small size of the gold target compared to the size of the substrate.



(a) Polyimide support width: 100 µm.



(b) Polyimide support width: 200 µm.



(c) Schematic representation of the cross sections indicated in (a) and (b).

Figure 3.19: Zoomed view of 100 µm wide horseshoe shaped gold conductors, encapsulated in PDMS and supported by 100 µm and 200 µm wide polyimide.

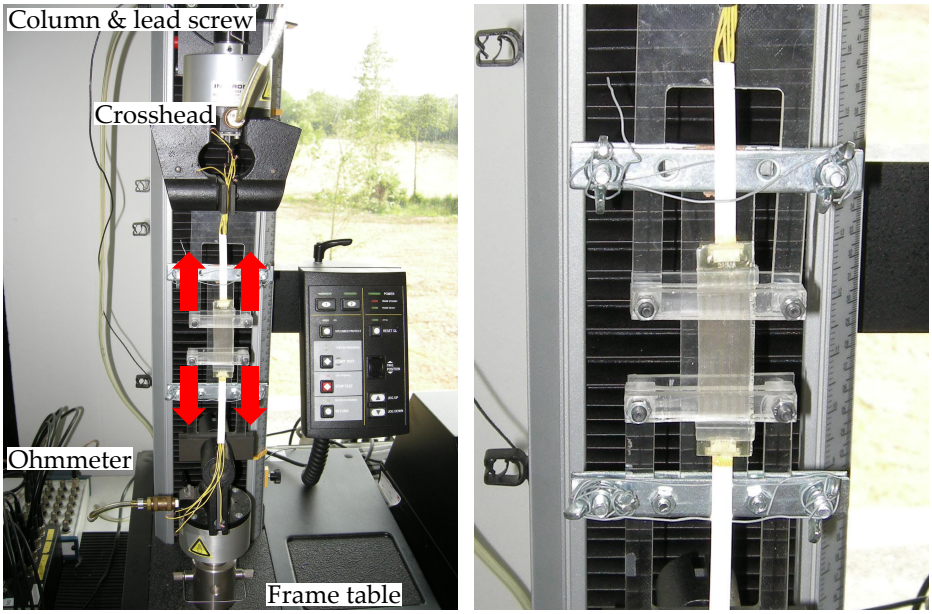
3.3.3 Mechanical performance

Test setup

The horseshoe shaped interconnections are stretched using an Instron 5543 load frame (Figure 3.20(a)) [20]. These load frames are designed to test a wide range of materials at various loads. As indicated in Figure 3.20(a), a crosshead is mounted on a column and lead screw. By rotation, the lead screw is able to drive the crosshead up or down the column and as such applies load to the material specimen which is fixed between the frame table and the crosshead. A load cell, secured to the crosshead, measures the resulting load on the material specimen. Together with an ohmmeter, the load frame allows for automated data collection (electrical resistance versus strain and time) of four interconnections simultaneously.
The samples are clamped by means of a dedicated clamping tool which minimizes the orthogonal force onto the sample. Therefore, two filleted pieces of PDMS are introduced along the thickness of the sample, as noticed on the left and right side of the sample displayed in Figure 3.15(a). These filleted pieces of PDMS are realized during injection molding in case of molded samples (as is the case for Figure 3.15(a)), or by plasma bonding such an individual molded piece on top of the sample in case of spin coated samples. These thicker PDMS parts are subsequently used to fixate the sample into the dedicated clamping tool as illustrated in Figure 3.20(b); the sample can thus still quite freely move within the clamping tool (e.g. transversal contraction caused by the Poisson's effect), thereby minimizing the effect of clamping on the electrical response. Also notice that the clamping is done so that the ZIF sockets do not affect the mechanical performance of the horseshoe shaped interconnections.

One-time uniaxial stretching

In Figure 3.21, the course of the electrical resistance of each horseshoe shaped interconnection type ((a) 100 µm and (b) 200 µm polyimide support width) is represented during uniaxial stretching up to two times the original length (strain of 100 %) at a strain rate of 1 %/s. The initial electrical resistance of both tracks was 181 Ω. During stretching, the electrical resistance which is represented in Figure 3.21(b) shows minor variations. It has to be noted that the signal conditioning superposes a ripple with a frequency of approximately 1.1 MHz on top of the actual signal, which results in 7 Ω resistance variation and as such reduces the measurement precision. This is clearly illustrated in Figure 3.22 which represents the measurement of an electrical resistor with a fixed value of 180 Ω. The variations in Figure 3.21(b) thus fall within the measurement precision of the setup. It is quite clear though that the interconnection type which is represented by Figure 3.21(a) suffers from a slight increase in electrical resistance. Optical microscopy after and even during stretching does not indicate why this increase occurs. Hence, this be-



(a) Instron 5543 load frame.

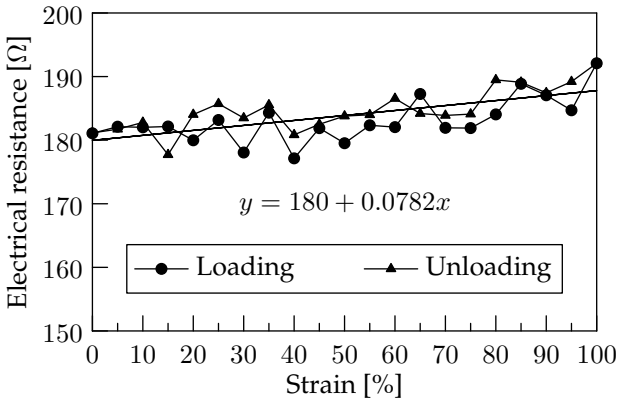
(b) Test structures loaded in the dedicated clamping tool.

Figure 3.20: Horseshoe shaped interconnections are stretched using an Instron 5543 load frame.

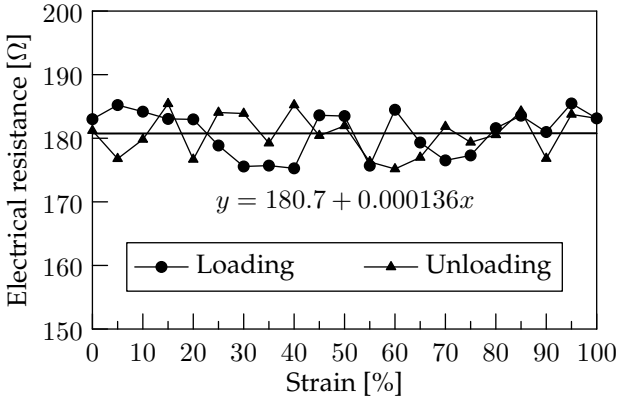
havior is not elucidated. It can be concluded that both types of interconnections (100 µm and 200 µm polyimide support width) stay highly conductive at strains up to 100 %. As the strain is released, the initial electrical resistance is recovered.

Cyclic mechanical loading

The lifetime of the horseshoe shaped interconnection types (100 µm and 200 µm polyimide support width) is evaluated by subjecting a limited number of fabricated test structures (two of each type) to various uniaxial strains for an extended period of time. The applied strains were chosen arbitrarily and thus solely serve as a means to demonstrate the cyclic mechanical performance of the interconnections. The strain rate was kept constant at 10 %/s during the different tests.
An example of the electrical resistance of a horseshoe shaped interconnection, cyclically stretched at 20 % strain, as a function of the number of straining cycles is shown in Figure 3.23. It has to be noted that the maximum electrical resistance which the ohmmeter can measure is capped at 414 Ω. The value of 414 Ω in the graph was actually verified to correspond with a failed interconnection, i.e. an infinite resistance. It is also observed that the electrical resistance remains stable until failure; no increase in electrical resistance is noticed.
The average number of cycles before electrical failure is graphically represented in Figure 3.24. It is seen that, as the elongation increases, the lifetime of the stretchable interconnections drops drastically. This can be explained by the accumulated plastic strain in the metal. Increasing the elongation results in more accumulated plastic strain in the metallic conductor. When the accumulated plastic strain in the metal reaches the intrinsic fracture strain, cracks are initiated, and eventually, the metal ruptures.
From Figure 3.24, it is clear that the width of the polyimide support has a great impact on the lifetime of the stretchable interconnections. This is clearly seen at the higher strains of 40 % and 60 % where the average number of cycles before electrical failure for conductors with the 200 µm support width (X) surpasses that of the conductors with 100 µm support width (Y) by a factor (X/Y) 170 and 255, respectively. It has to be noted that at these high strains, the PDMS in which the interconnections are encapsulated ruptured. The lifetime of the tracks with 200 µm support width mentioned for these strains thus actually indicate electrical failure of the tracks due to rupture of the PDMS. This is attributed to the manual cutting of the test structures which introduced imperfections at the edges of the PDMS encapsulant.
At the lower strains, the interconnections have an increased lifetime. At 20 % strain, a similar trend as for the higher strains is noticed; at 10 % strain, both interconnection types have a lifetime exceeding 500 000 cycles, with a hardly measurable change in resistance. The tests at these lower strains were eventually stopped at 500 000 cycles without clear indication that electrical failure would occur.



(a) Polyimide support width: 100 µm.



(b) Polyimide support width: 200 µm.

Figure 3.21: Electrical resistance of meandering horseshoe shaped interconnections with varying polyimide support width (100 µm and 200 µm), when uniaxially stretched up to 100 % at a strain rate of 1 %/s.

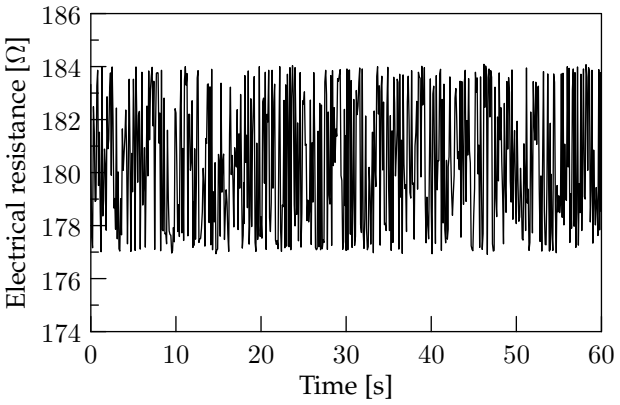


Figure 3.22: Electrical resistor with a fixed value of 180 Ω measured with the test setup (sampling frequency 10 Hz).

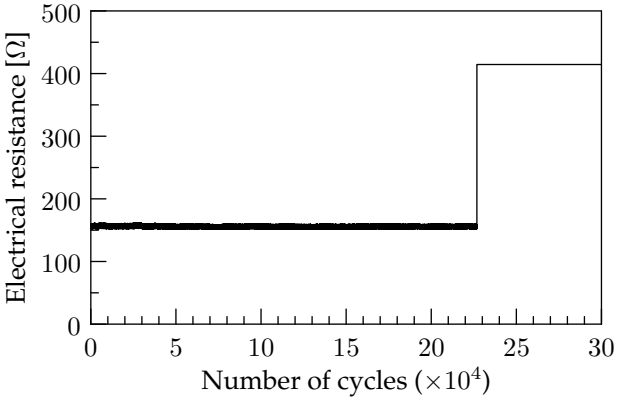


Figure 3.23: Electrical resistance of a horseshoe shaped interconnection, cyclically stretched at 20 % strain, as a function of the number of straining cycles.

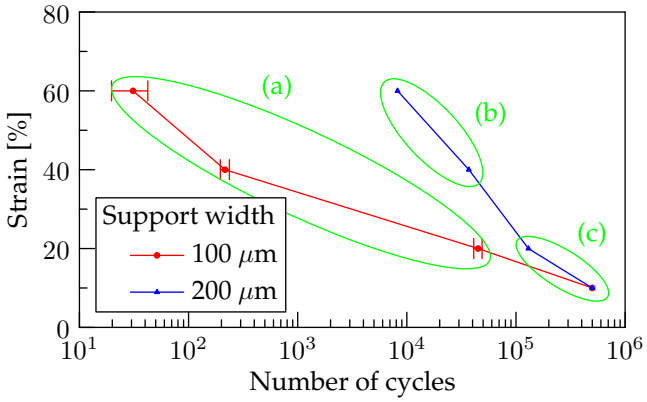


Figure 3.24: Average number of cycles before electrical failure of meandering horseshoe shaped gold conductors with varying polyimide support width when subjected to cyclic uniaxial strains. Three distinct regions are indicated: (a) interconnections stopped conducting, (b) rupture of the PDMS and (c) interconnections still conducting when the test was stopped. The error bars represent the standard deviation s of the sample consisting of two measurements.

Considering the large number of straining cycles before electrical failure at the lower strains, it is expected that the failure mechanism is governed by high-cycle fatigue (Section 2.2.2). However, because of the large number of cycles, but also because the interconnections are fully encapsulated in PDMS, a detailed analysis (e.g. by SEM) of the metallic conductors was not conducted as this was not feasible. The failure mechanisms are thus not elucidated.

3.4 Conclusions

A new fabrication technology for stretchable electrical interconnections has been presented. These are realized by patterning a 200 nm thick sputter deposited gold film into meandering horseshoe shapes, and covering by polyimide PI-2611 as a means to improve the mechanical performance. The polyimide is patterned by dry etching; optimization through the Taguchi methodology is illustrated.

The processing of the stretchable interconnections is performed on glass substrates; they are encapsulated in a silicone elastomer in a final stage. To this end, a customized release technique compatible with high temperatures up to 350 °C is developed based on the evaporation of a 400 nm thick layer of potassium chloride. Horseshoe shaped conductors with a track width down to 20 µm

were encapsulated in a silicone elastomer. This approach allows the use of diverse types of silicone elastomers (e.g. biomedical grade) or other elastomers (e.g. polyurethanes).
The technology was demonstrated by fabricating two versions of test structures consisting of horseshoe shaped gold conductors designed along straight parallel lines in between test pads. The track width of the gold conductors was fixed at 100 µm, and these were alternately covered by polyimide support with widths of 100 µm and 200 µm. For one version, off-the-shelf ZIF sockets were mounted on separated polyimide islands which are interconnected by stretchable wiring and encapsulated in PDMS; the other version solely consisted of stretchable interconnections. The resulting encapsulated circuits are both highly conformable and stretchable.
Reversible stretching of the test structures at uniaxial strains up to 100 % was illustrated. Cyclic mechanical loading of the test structures clearly highlighted the impact of the polyimide support width on the reliability. Stretchable interconnections composed of polyimide support which is 100 µm wider than the gold conductor were found to have a greatly increased lifetime compared to interconnections for which the polyimide support and gold conductor have an identical width. At high strains of 40 % and 60 %, the former remained highly conductive until the silicone elastomer ruptured, in contrast to the latter which failed at an earlier stage. Both interconnection types were found to have a lifetime of minimum 500 000 cycles at a strain of 10 %; no change in electrical resistance was noticed.

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4

Stretchable electronics platform using thin dies

4.1 Introduction

A general concept for realizing conformable, stretchable electronics consists in the use of the pixelated architecture presented in Chapter 2: various non-stretchable islands are connected by stretchable electrical wiring, which is able to deform with the elastomeric substrate. The islands are composed of a structural polymer, and are designed to host fragile devices (e.g. traditional, rigid electronic components).
In Chapter 3, the fabrication and evaluation of the stretchable electrical wiring is presented. Special attention was given to improve the mechanical performance by covering the interconnections with polyimide. Furthermore, test structures were fabricated with off-the-shelf ZIF sockets assembled on separated polyimide islands, illustrating the pixelated architecture concept.
To improve the overall mechanical flexibility and conformability, it is clear that a certain degree of flexibility in the islands is also desired. An elementary result in mechanics is exploited: common electronic materials, or any material for that matter, become flexible if sufficiently thinned (Section 2.2.3). Therefore, focus is put on the implementation of active electronic components by embedding them as thin dies in a slim polyimide package (~50 µm - 60 µm).
In the first section of this chapter, the fabrication process is described in detail. Dies with thicknesses of both 20 µm and 30 µm are embedded in polyimide is-

lands, while the fan-out metallization is configured as polyimide covered meandering conductors. By subsequent encapsulation in PDMS, a system is achieved that can flex and stretch. The process is demonstrated using so-called daisy chain silicon dies, which allow for quantification of the contacting yield from the package to the die level. The remainder of the chapter deals with the evaluation of the test design.

4.2 Fabrication process

The fabrication process for the stretchable electronics platform using thin dies is described in detail, and demonstrated by embedding PTCE silicon dies (Section 4.3.1).

4.2.1 Overview

A schematic representation of the fabrication process is shown in Figure 4.1. Each step will be discussed in detail in the following, corresponding sections. The fabrication is started by cleaning a glass substrate (Figure 4.1(a)) and depositing a release stack (Figure 4.1(b)). Next, thinned dies are placed with the active side up (face-up) in between two spin-on polyimide films using a liquid adhesive (Figure 4.1(c) - Figure 4.1(e)). Vias are provided towards the die bond pads by dry etching (Figure 4.1(f) - Figure 4.1(i)), ENIG surface finish is performed (Figure 4.1(j)) and gold metallization is sputter deposited (Figure 4.1(k)). The metallization is patterned via photolithography (Figure 4.1(l)) and covered by depositing another polyimide film (Figure 4.1(m)). All polyimide films are then patterned in a single dry etch step to form polyimide covered meandering conductors and non-stretchable islands with embedded thinned dies (Figure 4.1(n) - Figure 4.1(q)). At a final stage of the fabrication process, the circuit is transferred to PDMS by a two-step embedding procedure (Figure 4.1(r) - Figure 4.1(s)).
To improve the clarity of this section, a unique name for each of the different layers of polyimide and PDMS is presented in Figure 4.2. This nomenclature will be used throughout the entire section.

4.2.2 Substrate

The substrate selection and cleaning are identical to those for the stretchable electrical interconnections, described in Section 3.2.2.

4.2.3 Release layer stack

As illustrated in the schematic representation of the fabrication process (Figure 4.1), the transfer to PDMS is performed at a final stage of the fabrication process. This requires the complete stack displayed in Figure 4.1(q) to be separated from

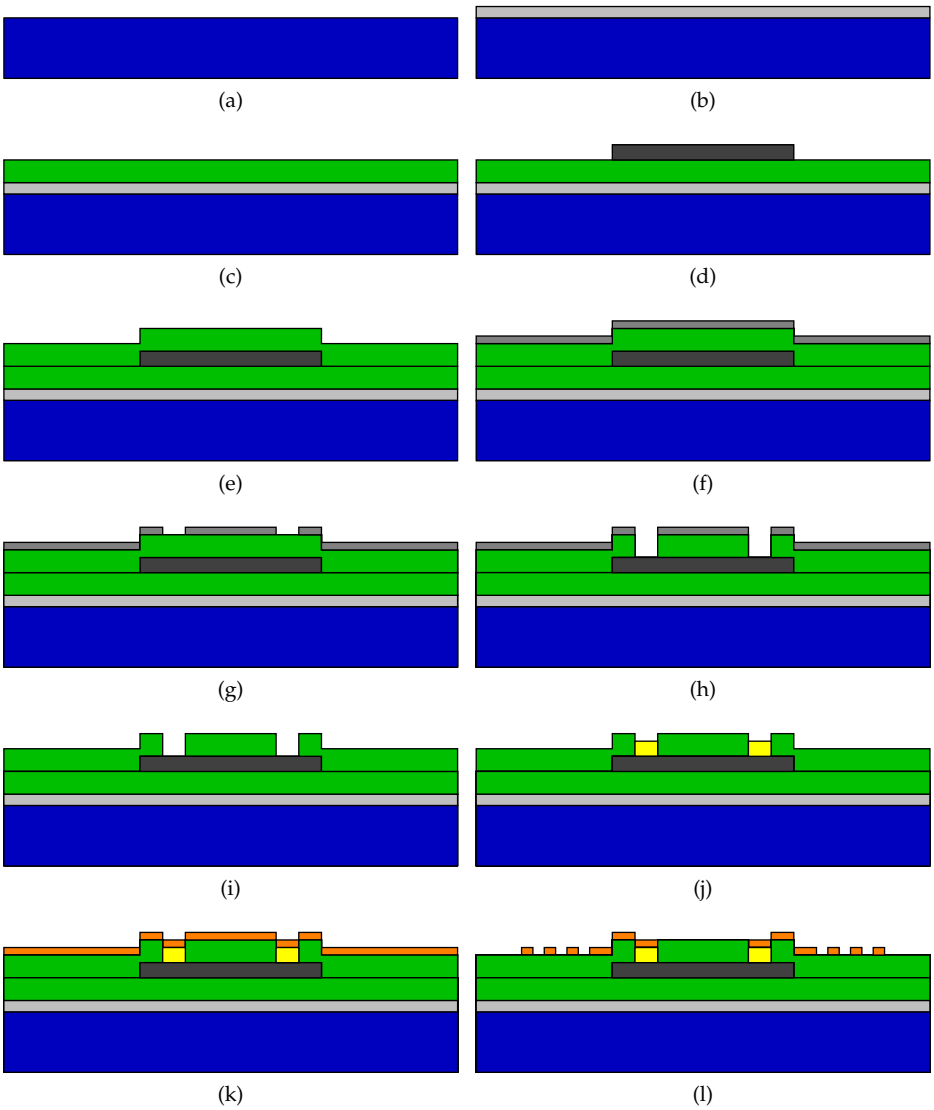


Figure 4.1: Fabrication process for stretchable electronics using thinned dies: cross-sectional views of the fabrication steps (not drawn to scale; a brief description is found in Section 4.2.1) - part 1.

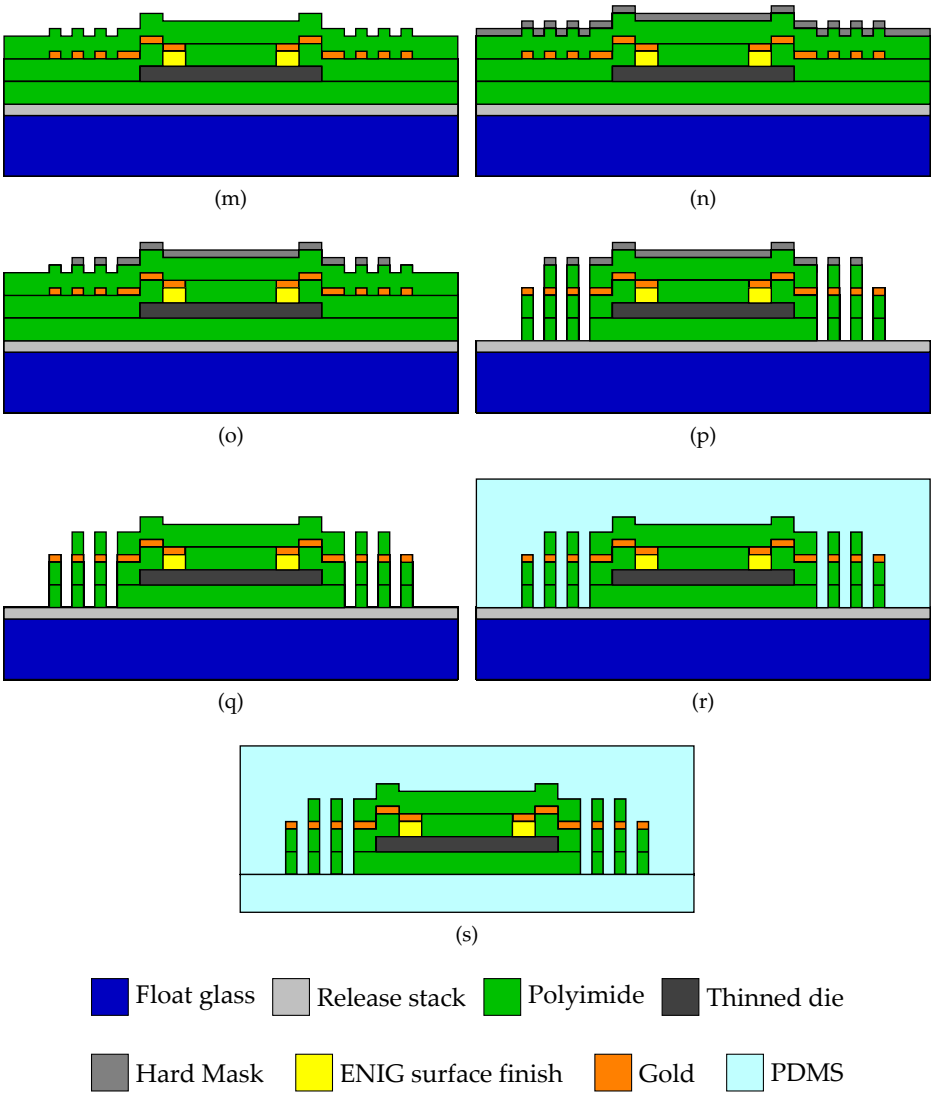


Figure 4.1: Fabrication process for stretchable electronics using thinned dies: cross-sectional views of the fabrication steps (not drawn to scale; a brief description is found in Section 4.2.1) - part 2.

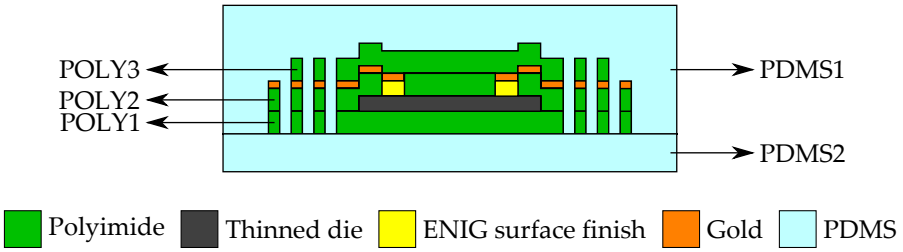


Figure 4.2: Stretchable electronics using thinned dies: nomenclature for the different layers of polyimide and PDMS (not drawn to scale).

the glass substrate and has been proved quite challenging due to the diverse processing conditions.

Selection criteria for the release procedure

The selection criteria for the release procedure are similar to those described in Section 3.2.3. As thin dies are present in the stack, it is emphasized that the release needs to be performed without exerting excessive force on, or bending of the stack. The latter could result in breakage of the thin die.

Customized release layer stack

The customized release layer stack described in Section 3.2.3 is copied without any adaptations (Table 4.1).

4.2.4 Application of PI-2611

During fabrication of the stretchable circuit, different layers of PI-2611 are deposited: a base layer (POLY1) on which the die is placed, a second layer (POLY2) to cover the thin die and in which vias are etched, and a final layer (POLY3) to cover the metallization. The polyimide layers are applied by the spin coat and cure procedures described in Section 3.2.4; identical parameters were chosen for each layer (Table 4.2).
In the following subsections, the different layers of PI-2611 will be shortly discussed as different pretreatments of the underlying layer are required, but also different criteria are used to evaluate the quality of the deposited film.

POLY1

The first layer of PI-2611 is spin coated on top of the 1 µm thick aluminium film which is part of the release layer stack (Figure 3.7). Although it is suggested to

Step #	Description	Parameters
(a)	Apply shadow mask	Al foil
	Evaporate KCl	Thickness: 400 nm,
	(Leybold Heraeus Univex 450)	Chamber pressure: 4×10^{-6} mbar,
		Deposition rate: 5 Å s^{-1}
	Remove shadow mask	
(b)	Apply PI-2611	See Table 4.2
(c)	Sputter deposit TiW	Thickness: 20 nm,
	(Leybold Z550)	DC power: 1200 W,
		Chamber pressure: 1×10^{-2} mbar
	Sputter deposit Al	Thickness: 1 µm,
	(Leybold Z550)	DC power: 2000 W,
		Chamber pressure: 2×10^{-3} mbar

Table 4.1: Process parameters for the application of the customized release layer stack.

Step #	Description	Parameters
(a)	Manual, static dispense	Approximately 1 ml
(b)	Spin coat	Start at 500 rpm,
		Hold 5 s at 500 rpm,
		Ramp to 3000 rpm at 250 rpm s^{-1},
		Hold 30 s at 3000 rpm
(c)	Bake	Hotplate, 10 min at 200 °C
(d)	Final cure	Ramp to 200 °C at 4 °C min^{-1},
	(inert atmosphere)	Hold 30 min at 200 °C,
		Ramp to 350 °C at 2.5 °C min^{-1},
		Hold 60 min at 350 °C,
		Gradually cool to RT

Table 4.2: Process parameters for the application of PI-2611.

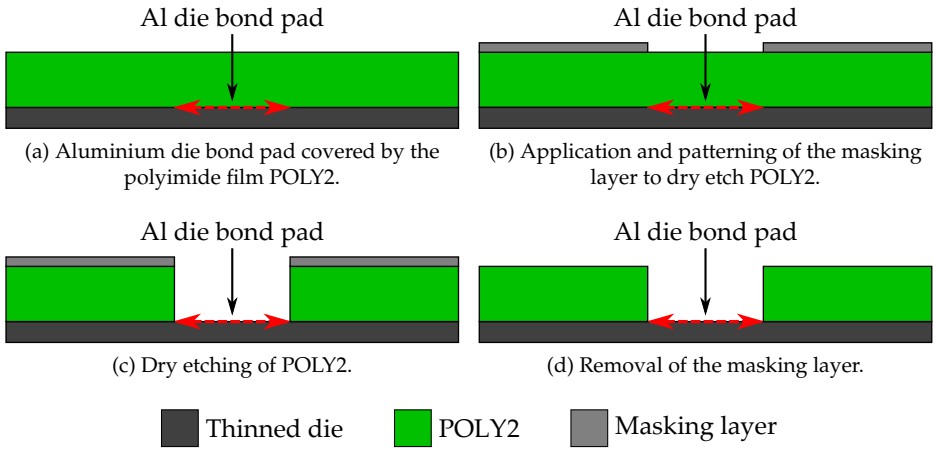
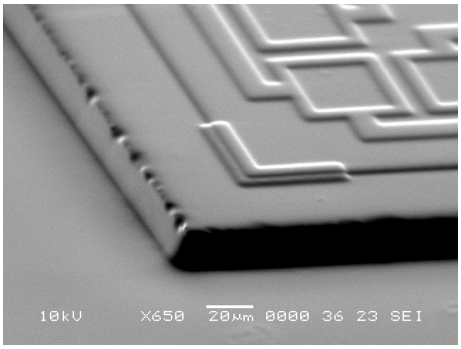


Figure 4.3: Cross-sectional views of the fabrication steps to provide vias towards the aluminium die bond pads (not drawn to scale).

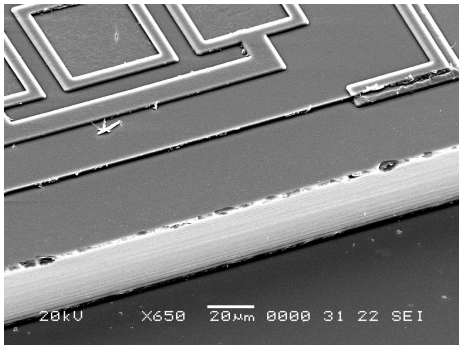
use an aminosilane based adhesion promoter such as VM-651 or VM-652 (HD Microsystems^{TM}) to enhance adhesion on materials like silicon, ceramic and metals, it was found unnecessary as sufficient adhesion is readily obtained.

POLY2

The second polyimide film covers the thin die before applying metallization. Its thickness is limited because of two closely related reasons. (a) Vias towards the die are provided by dry etching (Section 4.2.6). To restrain the etch time, the height of the vias (or the thickness of POLY2) is limited. (b) As will be discussed in Section 4.2.6, a masking layer is required to pattern the PI-2611 film by dry etching. A patterned aluminium film is frequently used for this purpose since it is inert for the oxygen (O_2) and trifluoromethane (CHF_3) chemistry used to etch PI-2611. After dry etching, the masking layer is completely removed by wet etching. However, the bond pads of the dies are frequently composed of aluminium (e.g. the PTCE dies), rendering the use of an aluminium hard mask incompatible with the process. This is schematically illustrated in Figure 4.3: an aluminium hard mask renders the selective removal of the masking layer (Figure 4.3(d)) impossible without additional efforts. Therefore, a patterned titanium tungsten film is used as masking layer to etch the vias. In contrast to aluminium, titanium tungsten is not inert for the used etch chemistry. It is etched at a much smaller rate than PI-2611, but anyhow limits the height of the vias to be etched (or the thickness of POLY2).



(a) 20 µm thick PTCE die; covered by a 5.5 µm thick polyimide film.



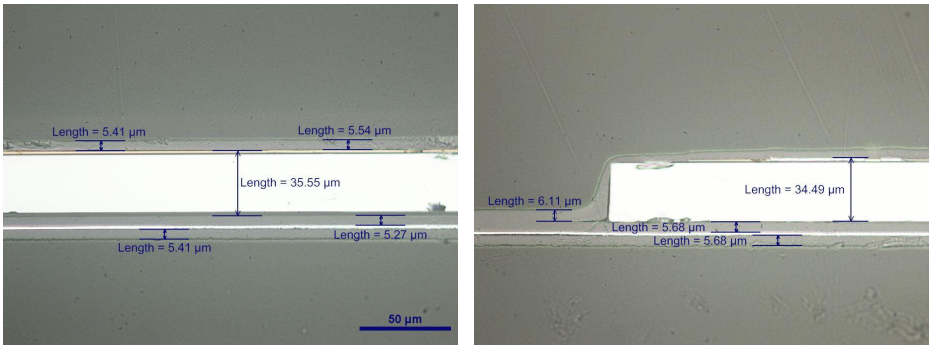
(b) 30 µm thick PTCE die; not covered.

Figure 4.4: SEM images of the edges of thin PTCE dies.

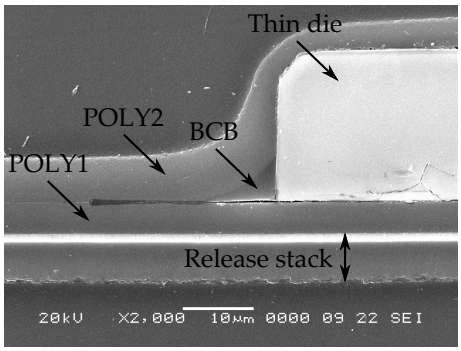
Keeping these two limiting factors in mind, a thickness of 5.5 µm is proposed for the covering polyimide film POLY2. As this is a factor 4 to 6 thinner than the thin die, the continuity of the cured polyimide film POLY2 was inspected, particularly at the edges of the thin die. The edges were visualized by SEM (Figure 4.4(a)), but it was difficult to take a conclusion about the continuity. However, the images gave us the impression that the step coverage is okay. Cross sections of embedded dies confirmed this impression; these are displayed in Figure 4.5 for a 30 µm thick die. Note that the rugged edge in Figure 4.4 is caused by imperfections at the edge of the die due to the dicing. These imperfections are clearly noticed in Figure 4.4(b).
To improve the adhesion to the thin die, a thin layer of the aminosilane based adhesion promoter VM-652 is applied. This is done by spin coating at 3000 rpm for 30 s, followed by a baking step on a hotplate for 1 min at 120 °C. Primed substrates are not stored; the polyimide coating is applied as soon as possible. Furthermore, to improve the adhesion to POLY1, its surface can be slightly roughened prior to application of the adhesion promoter, according to the procedure described for POLY3. However, this was found unnecessary as no adhesion problems were noticed.

POLY3

The third coating of polyimide is less critical as its sole purpose is to cover the gold metallization. To improve the adhesion to POLY2, the surface of POLY2 is slightly roughened by exposing it briefly for 1 min to an oxygen (O_2) plasma prior to the application of POLY3. A System VII Batchtop RIE (Plasma-Therm) is used for this purpose with following parameters: RF power 150 W, O_2 flow rate



(a) (b)



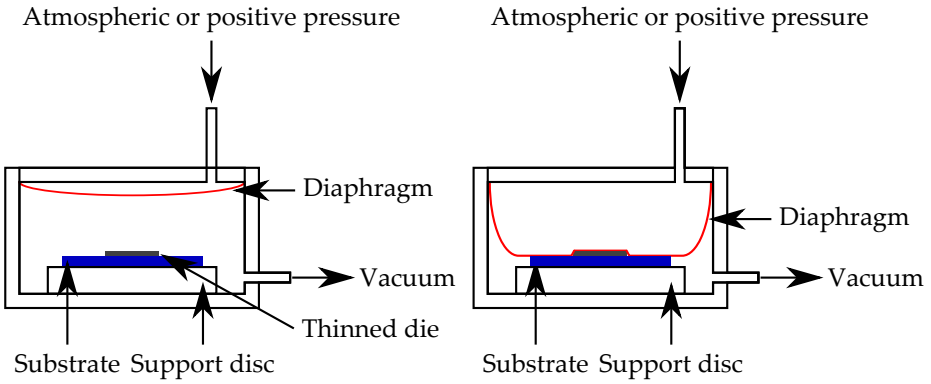
(c)

Figure 4.5: Cross sections of a 30 µm thick PTCE die covered by a 5.5 µm thick PI-2611 film, indicating the thicknesses of the different polyimide films and illustrating the continuity of the polyimide coatings at the edges of the die.

25 sccm and chamber pressure 150 mTorr.

4.2.5 Placement of thin dies

The thin dies are placed with the active side up (face-up) on the first polyimide film POLY1. As thinning reduces the rigidity of the die, it often produces large warpage caused by residual stress of the surface films (e.g. multilayer metal stacks, dielectric materials). Therefore, care is taken to place the thin dies flatly, but also to avoid the presence of voids between the die and the adhesive. This is required in order to avoid breakage of the die and dimensional errors during subsequent processing, e.g. during photolithography which requires close contact between the substrate/die assembly and the glass mask, possibly causing breakage or deformation of the die.
After placement of the thin dies, two layers of polyimide PI-2611 still have to be spin coated and cured. Therefore, it is important to choose an adhesive which is compatible with the corresponding high-temperature curing profile (Table 4.2). This requirement limits the amount of adhesives greatly. In previous work, the polyimides PI-2610 and PI-2611, and diverse formulations of the CYCLOTENE^{TM} 3000 series (The Dow Chemical Company), which are resins derived from B-staged bisbenzocyclobutene (BCB) monomers, were considered as adhesive [1, 2]. It was reported that the use of polyimides is not advisable due to outgassing of residual solvents and by-products during cure, causing voids between the adhesive and the die. The CYCLOTENE^{TM} resins on the other hand are more suited since outgassing of solvents occurs at an early stage, while no volatiles evolve during cure.
The low viscous CYCLOTENE^{TM} 3022-46 resin is selected as liquid adhesive. A small volume (droplet) is manually deposited by means of a syringe on the base PI-2611 film at the position the die should be fixated. The droplet is then baked on a hotplate for 2 min at 100 °C to remove the solvents. The temperature and time for this bake are actually not critical: the temperature can be set from 80 °C to 150 °C and the time can be as short as 60 s. The thinned die is then carefully positioned on the baked droplet with its active side up (face-up) and the assembly is placed in a WSB2 wafer substrate bonding unit (Logitech). The bonding head of this unit consists of 2 chambers: a sample chamber which can be evacuated to beyond 0.1 mbar and an upper diaphragm chamber. Both chambers are separated by a flexible diaphragm as depicted in Figure 4.6(a). The "heat and outgas"-program is used to bond the assembly. At the start, air is evacuated from the upper diaphragm chamber and then from the sample chamber. Once the sample chamber is evacuated, its temperature is raised to 150 °C to soften the adhesive droplet. After a soak of 10 min to allow equalization of the temperature throughout the bonding head and the substrate, but also to allow outgassing of the adhesive, a moderate pressure of 500 mbar is admitted to the space above the flexible diaphragm, allowing the diaphragm to drop and press the die into



(a) Sample loading (diaphragm up). (b) Bonding of the die (diaphragm down).

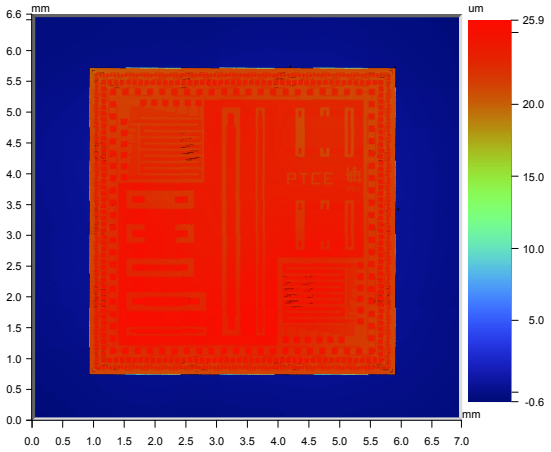
Figure 4.6: Cross section of the bonding head of a WSB2 wafer substrate bonding unit.

the adhesive (Figure 4.6(b)). The pressure is maintained for 30 min before gradually cooling the assembly to room temperature, resulting in flatly placed thin dies without the presence of voids.

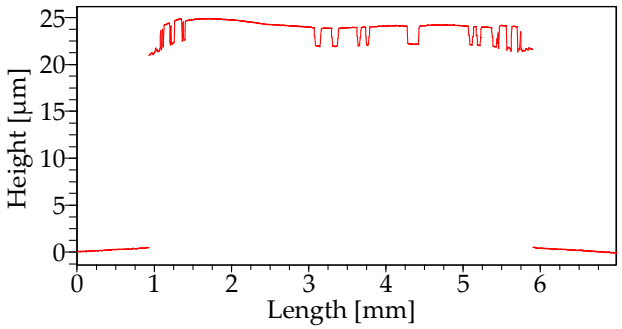
A surface scan of a placed thin die, taken using an optical profiler WYKO NT3300 (Veeco), is shown in Figure 4.7(a). As noticed, the BCB / thin die assembly has a thickness of approximately 26.5 µm. In Figure 4.7(b) and Figure 4.7(c), the cross-sectional profiles are displayed along the horizontal and vertical centerline, respectively. Thickness variations of maximum ~3 µm are noticed.

A common problem caused by the use of liquid adhesives is surface contamination of the die: the adhesive material flows onto the die surface because it is softened and squeezed during bonding. The degree of surface contamination is determined mainly by the volume of the adhesive material droplet and the exerted pressure during bonding. In Figure 4.8(a), a typical example of surface contamination of a thinned die is displayed. Because the BCB has been only partially cured up to this point (40 min at 150 °C, see Figure 4.9), it can still be removed with an appropriate solvent. In the product data sheet, immersion in T1100 solvent is recommended [3]. However, in this work the surface was cleaned by wiping the surface with acetone, followed by immersion in a bath of IPA and DI. The cleaned surface is displayed in Figure 4.8(b).

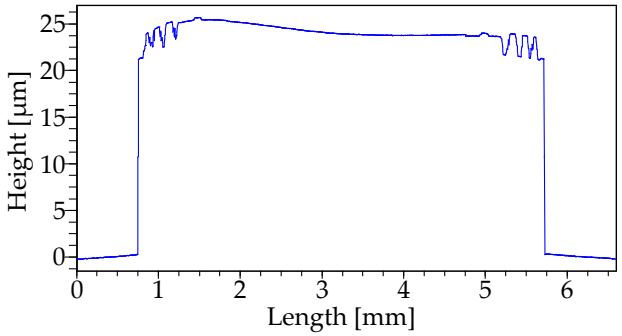
Finally, the CYCLOTENE^{TM} 3022-46 is fully cured. As the resin is susceptible to oxidation at elevated temperatures ($\geq$150 °C), it is cured in a nitrogen flushed oven. The curing profile resembles the curing profile of PI-2611 and is described in detail in Table 4.3. Taking a closer look at the data presented in Figure 4.9, it is clear that the curing profile results in a full cure of the adhesive.



(a) Overview.

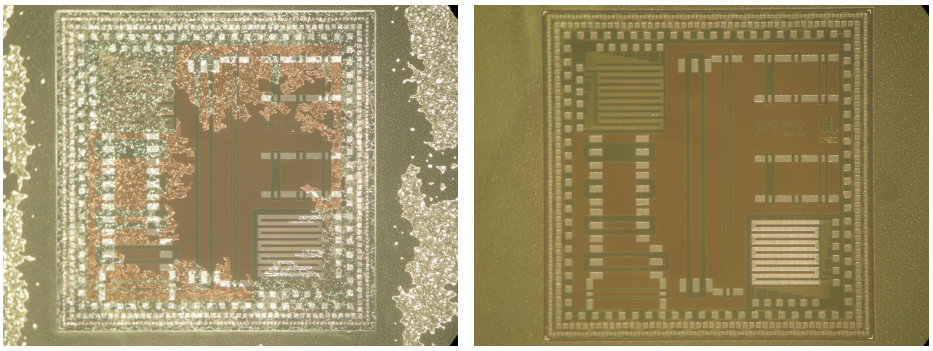


(b) Cross-sectional profile along the horizontal centerline.



(c) Cross-sectional profile along the vertical centerline.

Figure 4.7: Surface scan of flatly placed thin dies.



(a) Before excess adhesive removal. (b) After excess adhesive removal.

Figure 4.8: Thinned PTCE die (20 µm thickness) fixated on a base polyimide film by means of CYCLOTENE^{TM} 3022-46 resin.

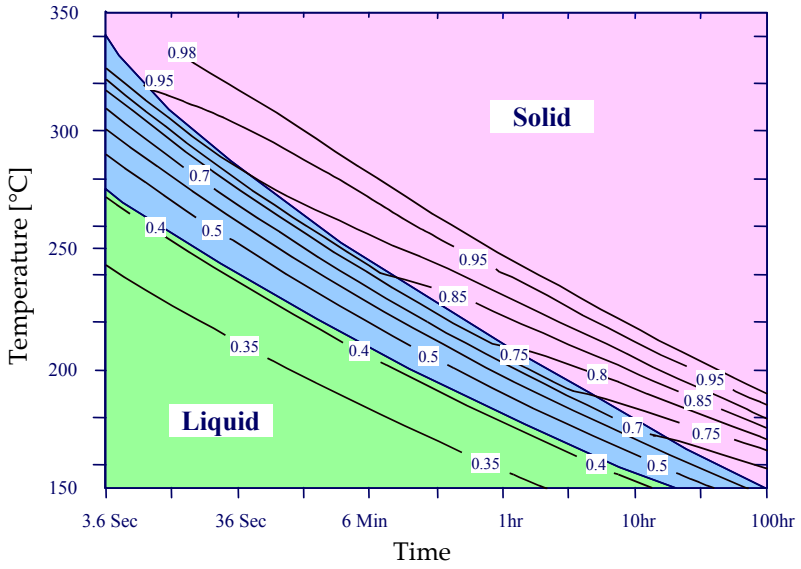


Figure 4.9: The extent of BCB cure as a function of temperature and time [3].

Step #	Description	Parameters
(a)	Manual dispense of adhesive	Droplet of CYCLOTENE^{TM} 3022-46
(b)	Bake	Hotplate, 2 min at 100 °C
(c)	Die placement	Face-up on adhesive droplet
	Wafer substrate bonder	Evacuate air from the chambers, Ramp to 150 °C, Hold for 10 min at 150 °C, Membrane pressure: 500 mbar, Hold for 30 min at 150 °C, Gradually cool to RT
(d)	Remove excess adhesive	Wipe with acetone
	IPA rinse	2 min
	DI rinse	2 min
(e)	Final cure (inert atmosphere)	Ramp to 150 °C at 4 °C min^{-1}, Hold 30 min at 150 °C, Ramp to 250 °C at 2.5 °C min^{-1}, Hold 120 min at 250 °C, Gradually cool to RT

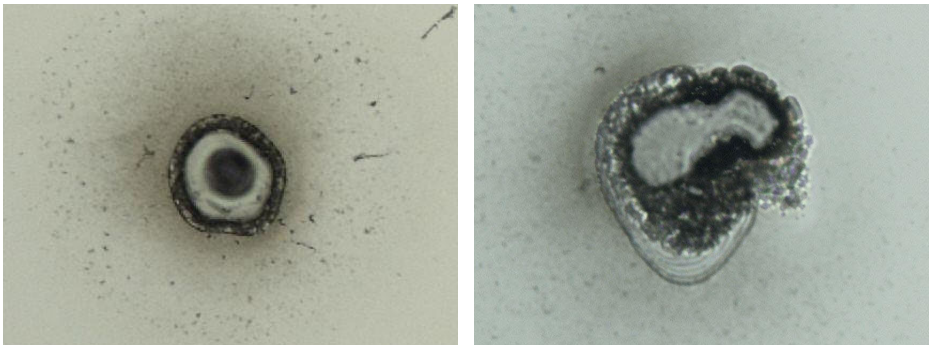
Table 4.3: Process parameters for the placement of thinned dies.

4.2.6 Via formation

Once the die is embedded in between two polyimide films (Figure 4.1(e)), vias are provided towards the bond pads of the die. Both dry etch processes and laser ablation techniques are the preferred routes for patterning PI-2611, as patterning PI-2611 films using traditional wet etch techniques is difficult due to the molecular structure and inherent film density. Laser ablation of polyimide has been illustrated with CO_2 lasers which are known for their high average power and high drilling throughput, and UV lasers which are recognized for their high precision material removal and ability to drill the smallest vias [4]. In previous work, microvia drilling using a CO_2 laser (9 µm - 11 µm), KrF excimer laser (248 nm) and Nd-YAG laser (355 nm) was considered [1, 2]. Using these laser drilling processes, one has to consider the minimum achievable feature sizes, re-deposition of the ablation products (debris), but also the ablation selectivity to the material underlying the polyimide, in this case the aluminium bond pads.
In the frame of this PhD research, tests performed with a 10.6 µm CO_2 laser illustrated that this type of laser is not suitable for high quality micropatterning. The high power and photothermal processes caused high structure roughness, the ablation quality and reproducibility was highly dependent on the precise focus depth of the laser, the ablation of vertical sidewalls was not possible, and the minimum achievable via sizes were limited to ~90 µm. In Figure 4.10, two vias are shown which were ablated using identical ablation parameters, but the ablation of the via displayed in Figure 4.10(b) was performed while the laser was slightly out of focus. Furthermore, it was found that a very thin residual polymer film remains on top of the underlying metal which cannot be removed using solely the CO_2 laser. When using lasers in the UV-range, on the other hand, it is generally more difficult to selectively ablate polymers on top of a thin metal film. Test were performed both with a 355 nm Nd-YAG laser and a 248 nm KrF excimer laser. Due to the Gaussian beam intensity profile of the former laser, it was found impossible to avoid damaging the underlying thin metal film at the center of the beam. Beam shaping is often used to avoid this problem and obtain a near-uniform irradiation profile, however, this was not investigated in this work. For the latter type of laser, the process window was found too small to effectively use this laser for via formation. Therefore, in this work, vias towards the bond pads are provided using a dry etch process. This choice was also partially motivated because a dry etch process is required to introduce the stretchability at a later stage, as illustrated in Figure 4.1(q) and discussed in Section 4.2.9.

Masking layer

An etch mask is required to pattern the PI-2611 film POLY2 by dry etching. A sputter deposited aluminium film, patterned by photolithography and wet etching, is frequently used for this purpose since it is inert for the oxygen (O_2) and trifluoromethane (CHF_3) chemistry used to etch PI-2611. After dry etch, the alu-



(a) CO_2 laser in focus. (b) CO_2 laser slightly out of focus.

Figure 4.10: The importance of the focus depth of the CO_2 laser during ablation of vias in a 5.5 µm thick PI-2611 film; the magnification of the optical microscope was identical for both figures.

minium film is completely removed by wet etching. However, the bond pads of the dies are also composed of aluminium, rendering the use of an aluminium hard mask incompatible with the process. Note that aluminium is used as a dry etch mask in a later stage of the fabrication process (Figure 4.1(q)).

Alternatively, also patterned copper and titanium tungsten were considered as dry etch mask since these metals were available for sputter deposition. Copper is inert for the used dry etch chemistry, though the copper etchants (solutions of $CuCl_2$ or $FeCl_3$) were found to harm the aluminium bond pads. Titanium tungsten on the other hand is not inert for the dry etch chemistry. It is etched at a much smaller rate than PI-2611 (an order of magnitude 10 less), and its etchant does not harm the aluminium bond pads. Therefore, a patterned titanium tungsten film was investigated for use as dry etch mask.

Using a dry etch mask which is not inert for the dry etch chemistry implies a matching of its thickness to the height of the vias to be etched. Titanium tungsten films with several thicknesses were sputter deposited and patterned by photolithography and wet etching. The latter is performed in a 30 % H_2O_2 solution at 55 °C. It was found that films with thicknesses above 350 nm suffered from photoresist peeling during wet etch. Therefore, the thickness of the titanium tungsten film was fixed at 300 nm, implicitly limiting the height of the vias.

The 300 nm thick titanium tungsten film is patterned by photolithography and wet etching. To this end, a 6.2 µm thick layer of positive photoresist AZ 4562 is spin coated at 4000 rpm for 60 s, soft baked on a hotplate for 2 min at 90 °C, UV exposed for 17.5 s at 10 mW cm^{-2}, developed for 1 min in 50 % Microposit^{TM} developer and hard baked for 30 min in a convection oven at 120 °C. Aligning dur-

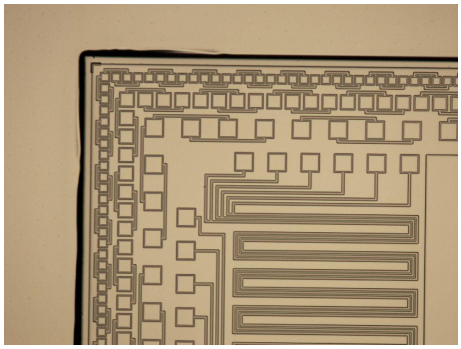


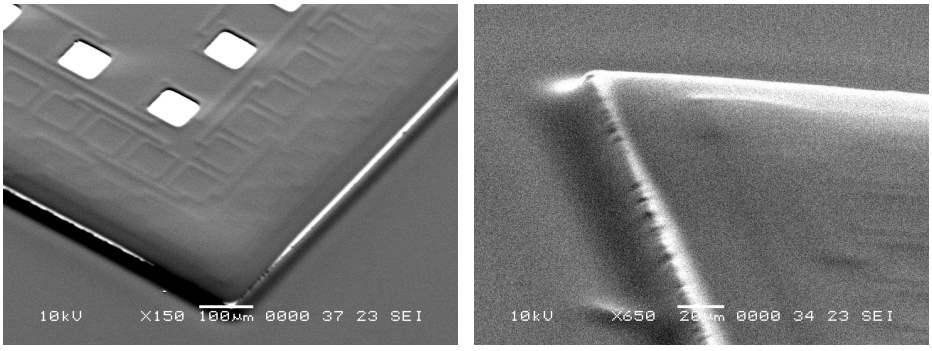
Figure 4.11: Bond pads of the die are visible through the 300 nm thick film of titanium tungsten.

ing photolithography is performed directly using the bond pads of the die which are visible through the 300 nm thick film of titanium tungsten, as illustrated in Figure 4.11. The metallization is then etched for 90 s in a 30 % H_2O_2 solution at 55 °C, followed by a 10 s rinse in a 30 % H_2O_2 solution at room temperature and rinse in deionized water. To enlarge the process window for the dry etching, the photoresist AZ 4562 is not stripped. Rather it is left on the titanium tungsten and functions as an extra masking layer. Note that photoresists typically have dry etch rates in the range of those of polyimides.

The use of a thick photoresist is not only advantageous because it is used as an extra masking layer for the dry etch, but it was also found necessary to obtain nice photolithography results. It is clear that covering the die with a single polyimide film results in height variations in the order of the thickness of the die. These non-uniformities result in a discontinuous photoresist coating at the edges of the die in case a 1.8 µm thick layer of photoresist S1818 is used. This is clearly illustrated in Figure 4.12. On the other hand, the use of a 6.2 µm thick layer of photoresist AZ 4562 effectively solves this problem, as illustrated in Figure 4.13. The importance of this continuous photoresist coating becomes clear when noted that it determines the continuity of the titanium tungsten dry etch mask, and consequently that of the PI-2611 film (Figure 4.14) and subsequent gold metallization (Figure 4.19).

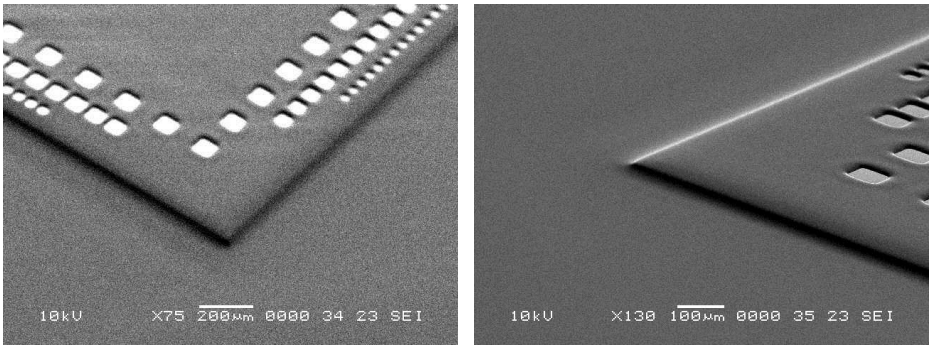
Dry etching

After applying the etch mask, the polyimide is dry etched for 21 min in a System VII Batchtop RIE (Plasma-Therm) using oxygen (O_2) and trifluoromethane (CHF_3) chemistry. The RF power, chamber pressure, O_2 and CHF_3 flow rate are fixed at 150 W, 150 mTorr, 15 sccm and 5 sccm, respectively. The parameters were



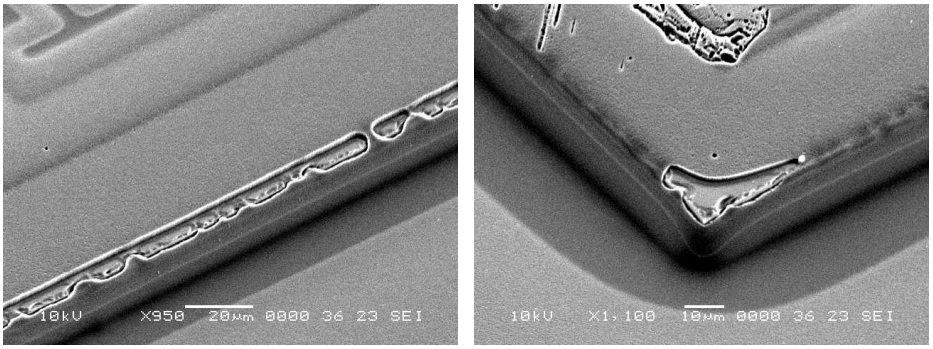
(a) (b)

Figure 4.12: The use of a 1.8 µm thick layer of photoresist S1818 to pattern the titanium tungsten etch mask results in a discontinuous coating at the edges of the die.



(a) (b)

Figure 4.13: The use of a 6.2 µm thick layer of photoresist AZ 4562 to pattern the titanium tungsten etch mask results in a continuous coating.



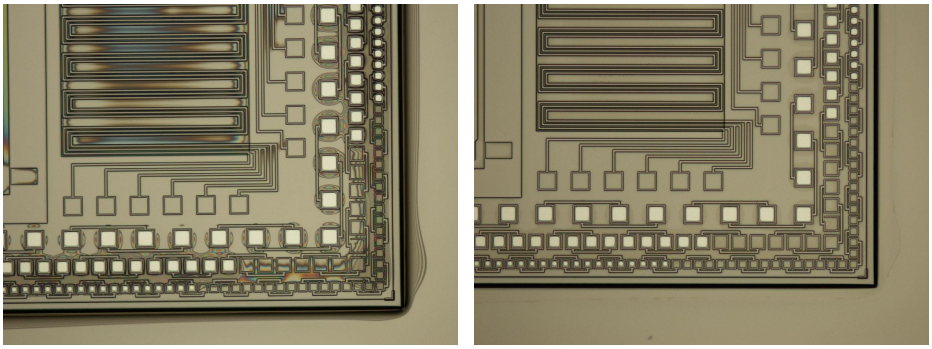
(a) (b)

Figure 4.14: The PI-2611 film at the edges of the die is dry etched due to a discontinuous photoresist coating and titanium tungsten film.

determined by an optimization through Taguchi methodology (Section 3.2.6). In Figure 4.15, it is illustrated that the stack of titanium tungsten and photoresist AZ 4562 effectively masks the PI-2611 film during the complete dry etch procedure. The mask was designed to provide square vias with side lengths ranging from 20 µm to 70 µm. A comparison with the glass mask for photolithography indicated that the side length of the vias defined in the photoresist AZ 4562 was approximately 3 µm larger (Figure 4.16(a)). After dry etch, another 1 µm to 2 µm was added to the side length of the vias (Figure 4.16(b)).

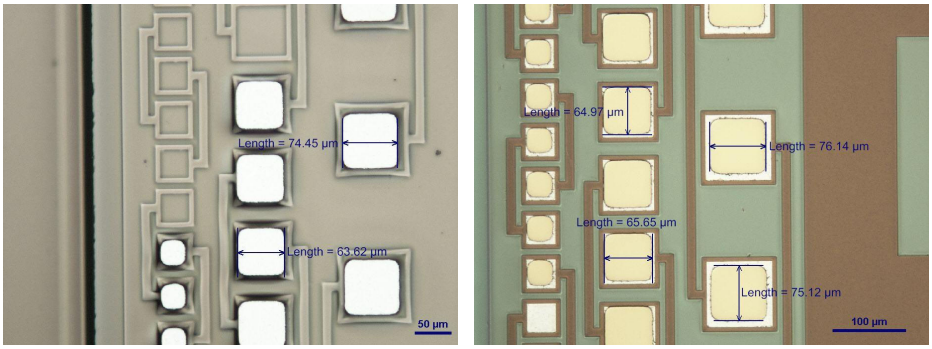
4.2.7 ENIG surface finish

The vias etched in the second polyimide layer POLY2 provide a means to electrically connect the die through its aluminium bond pads; this is schematically represented in Figure 4.17(a). Aluminium is the dominant material for IC bond pad metallization as it provides a satisfactory surface for conventional wire bonding. The electrically insulating aluminium oxide (Al_2O_3) which is formed immediately upon exposure to air does not cause a problem as the wire bond in its formation scrubs through the oxide to weld with the underlying metal. However, achieving a stable, low resistance electrical connection by sputter depositing another metal 'directly' on the bond pad requires an alternative strategy to deal with the tenacious oxide. Aside from the oxide, also the use of gold as material for metallization requires special attention. It is known that diffusion occurs at contacts between aluminium and gold exposed to high temperatures, causing the formation of intermetallic compounds such as Au_5Al_2 (white plague) and $AuAl_2$ (purple plague) which exhibit poor electrical conductivity and brittleness [5, 6].



(a) Before stripping AZ 4562. (b) After stripping AZ 4562.

Figure 4.15: The hard mask effectively masks the PI-2611 film during the complete dry etch procedure.

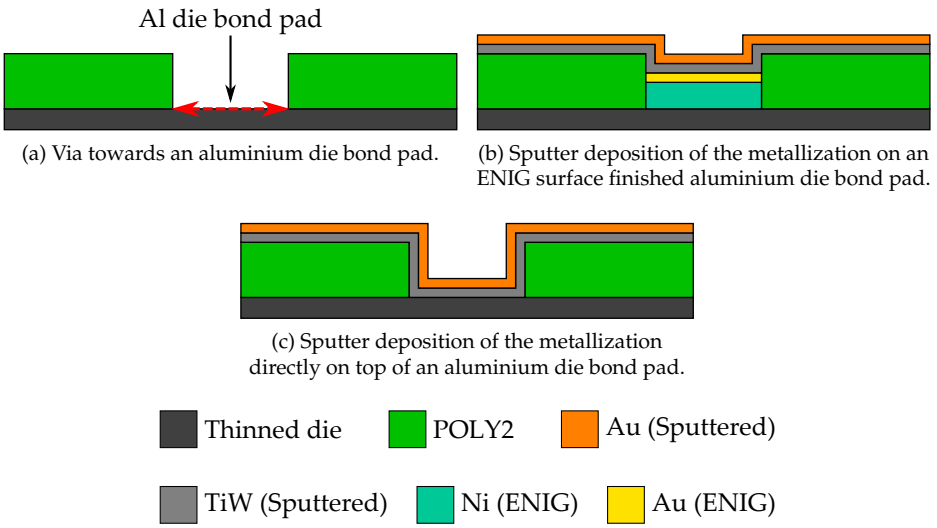


(a) Vias defined in AZ 4562. (b) Dry etched vias; ENIG surface finished.

Figure 4.16: Dimensions of the dry etched vias.

Step #	Description	Parameters
(a)	Sputter deposit TiW	Thickness: 300 nm,
	(Alcatel SCM600)	DC power: 1200 W,
		Chamber pressure: 1×10^{-2} mbar
(b)	Spin coat AZ 4562	60 s at 4000 rpm
	Soft bake	Hotplate, 2 min at 90 °C
	UV exposure	17.5 s at 10 mW cm^{-2}
	Development	50 % Microposit^{TM} developer, 1 min
	Hard bake	Convection oven, 30 min at 120 °C
(c)	Wet etch TiW	30 % H_2O_2, 90 s at 55 °C
		30 % H_2O_2, 10 s at RT
	DI rinse	2 min
(d)	Dry etch PI-2611	21 min,
	(System VII Batchtop RIE)	RF power: 150 W,
		Chamber pressure: 150 mTorr,
		O_2 flow rate: 15 sccm,
		CHF_3 flow rate: 5 sccm
(e)	Strip AZ 4562	Acetone, 2 min
	IPA rinse	2 min
	DI rinse	2 min
	Wet etch TiW	30 % H_2O_2, 90 s at 55 °C
		30 % H_2O_2, 10 s at RT
	DI rinse	2 min

Table 4.4: Process parameters for the via formation.



(a) Via towards an aluminium die bond pad.

(b) Sputter deposition of the metallization on an ENIG surface finished aluminium die bond pad.

(c) Sputter deposition of the metallization directly on top of an aluminium die bond pad.

Figure 4.17: Cross-sectional views of the different possibilities for metallization schemes towards the aluminium die bond pads (not drawn to scale).

Since the gold metallization is covered by applying another layer of PI-2611, the joints with the die would be subject to the high-temperature curing profile mentioned in Table 4.2.

To deal with the two issues mentioned previously, i.e. the aluminium oxide and the gold / aluminium diffusion, an electroless nickel immersion gold (ENIG) surface finish of the aluminium die bond pads is performed prior to the sputter deposition of the gold metallization (Figure 4.17(b)). During this process, the aluminium oxide is removed and a non-oxidizable gold surface finish, preceded by a nickel barrier layer, is provided. The nickel barrier layer ensures that the aluminium bond pads do not oxidize as the very thin immersion gold finish is typically not totally impervious. This barrier layer additionally prevents the occurrence of gold / aluminium diffusion, or diffusion of metals into the IC. The 50 nm thick titanium tungsten adhesion enhancement layer sputter deposited prior to the gold film, directly on the aluminium bond pad (as depicted in Figure 4.17(c)), was found ineffective to prevent gold / aluminium diffusion.

The ENIG surface finish is provided using a wet chemical process and requires the substrate to pass through a sequence of chemical baths. The patterned polyimide film POLY2 covering the die and providing vias towards the aluminium bond pads acts as a masking layer for the surface finish. Actually, electroless finishes do not require the use of a masking layer as they adhere only to the target metals on the die. However, the electroless nickel process is isotropic: the nickel

bump grows evenly in all directions. For tightly packed bond pads (i.e. small spacing), a masking layer such as the patterned polyimide can be used to guide the nickel growth and prevent shorts in between adjacent bond pads if the height of the nickel bump does not exceed the height of the vias. An additional benefit of the polyimide coating can be found in the shielding of the silicon substrate: for devices which contain bond pads in direct electrical contact with the silicon substrate, a galvanic cell can be created in the activation and plating solutions through contact with exposed areas of silicon [7]. This results in varied etching and deposition rates, leading to poor activation, damage to the bond pad, or an uneven plating thickness.

Electroless nickel plating of aluminium bond pads is not straightforward: direct plating of electroless nickel on aluminium is not reliable and leads to poor quality deposits with low adhesion. Therefore, to enable the nickel deposit to form a strong, electrically conductive bond with the aluminium, a number of cleaning and activation pretreatment steps are required; these are adopted from Hutt et al. [7]. The process is started by wetting the surface in deionized water and removing the aluminium oxide in a $50\,\mathrm{g\,l^{-1}}$ sodium hydroxide solution. The etch time, 20 s, is kept to a minimum to prevent excessive removal of aluminium from the bond pads. Aluminium is not normally used in its pure form, so depending on the alloy of aluminium, the surface of the bond pads can be covered in smut: the sodium hydroxide solution etches the aluminium and the oxide, but the other alloying materials are not removed and remain on the bond pad surface. Therefore, after a short rinse in deionized water, the substrate is dipped in a 37.9 % (m/m) nitric acid solution for 20 s to remove the non-aluminium constituents and organic residues, but not the aluminium. Another short rinse in deionized water ends the cleaning.

Next, the bond pad surface is activated by a zincate treatment: zinc coatings are very adherent, prevent the aluminium from reoxidizing and serve as an excellent seed layer for the electroless nickel plating. In this work, a double zincate treatment is performed as it has been reported that the double treatment results in more uniform zinc coatings and dramatic improvements in the adhesion of the nickel layer to the bond pads [7, 8]. The first zinc coating is applied by dipping the substrate in a 20 % (v/v) ALUMON^{TM} EN solution for 20 s; this dip also removes the aluminium oxide. The coating is then again removed by immersion in a 37.9 % (m/m) nitric acid solution for 20 s, and a second zinc coating is applied by dipping the substrate in a 20 % (v/v) ALUMON^{TM} EN solution for 20 s. In between each of the different steps, the substrate is rinsed in deionized water.

Nickel is then electroless plated on the zincate activated bond pads in two steps using commercial solutions. First, a nickel strike is applied using an ENPLATE^{TM} Al-100 solution (6 min at 38 °C), followed by the nickel plating in a MELPLATE^{TM} Ni 8600 solution (10 min at 85 °C). This should result in nickel deposit of approximately 3 µm thickness according to the product data sheet. Fresh solutions are prepared for every plating run, and a large object, i.e. a nickel surface of $20\,\mathrm{cm^2}$,

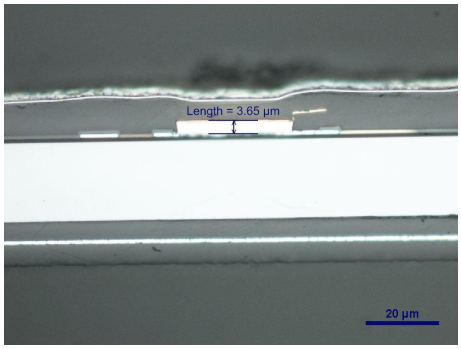


Figure 4.18: Cross section of a 20 µm thick die, at the stage of the fabrication process displayed in Figure 4.1(m), indicating the thickness of the ENIG surface finish.

is plated together with the substrates in order to comply with the recommended bath workload. This approach was suggested by Hutt et al. as it was reported that commercial nickel plating solutions can become over-stabilized during operation if the bath workload is not considered [9]. In case of the PTCE dies, the total bond pad area is approximately $1.002 \times 10^{-4}\,\mathrm{dm}^2$ and the volume of the solution was 1.8 l, while the MELPLATE^{TM} Ni 8600 solution is designed to operate with a nominal workload of $1.23\,\mathrm{dm}^2$ of surface area to be plated for every liter of solution.

Finally, a thin immersion gold coating is applied to prevent the nickel from oxidizing. This is done by immersing the nickel plated bond pads in an Aurolectroless SMT solution (8 min at 85 °C). According to the product data sheet, these parameters should result in a gold deposit with a thickness of approximately 60 nm. It should be remarked that in between every plating step, the substrate is rinsed in deionized water. Furthermore, all of the plating solutions are magnetically stirred in order to ensure a uniform temperature across the solution.

A cross section of an ENIG surface finished die bond pad is shown in Figure 4.18. Above-mentioned parameters result in an ENIG surface finish of approximately 3.6 µm thickness.

4.2.8 Metallization

After the bond pads are ENIG surface finished for reasons which are explained in Section 4.2.7, the metallization is applied.

Step #	Description	Parameters
(a)	DI soak	10 min
	Remove oxide	50 g l^{-1} NaOH, 20 s
	DI rinse	1 min
	Remove smut	37.9 % (m/m) HNO_3, 20 s
	DI rinse	1 min
(b)	Zincate activation	20 % (v/v) ALUMON^{TM} EN, 20 s
	DI rinse	1 min
	Strip Zn coating	37.9 % (m/m) HNO_3, 20 s
	DI rinse	1 min
	Zincate activation	20 % (v/v) ALUMON^{TM} EN, 20 s
	DI rinse	1 min
(c)	Electroless Ni strike	ENPLATE^{TM} Al-100, 6 min at 38 °C, Magnetically stirred
	DI rinse	1 min
	Electroless Ni plate	MELPLATE^{TM} Ni 8600, 10 min at 85 °C, Magnetically stirred
	DI rinse	1 min
(d)	Immersion Au coating	Aurolectroless SMT, 8 min at 85 °C, Magnetically stirred
	DI rinse	1 min

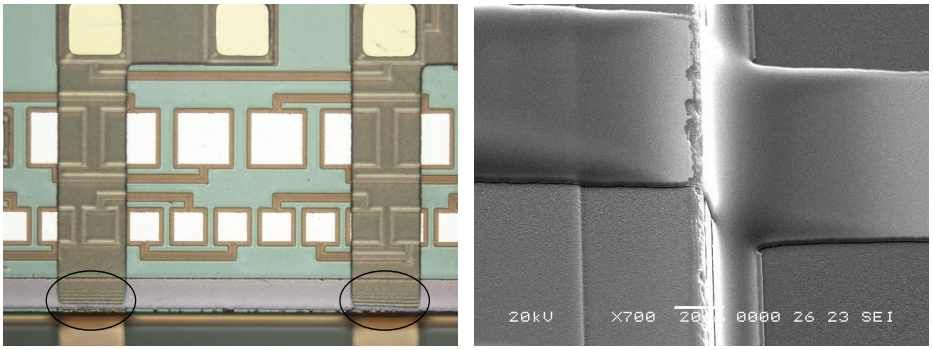
Table 4.5: Process parameters for the ENIG surface finish.

Sputter deposition

The metallization is deposited by DC magnetron sputtering in an Alcatel SCM600 system. A 200 nm thick gold layer and a 50 nm thick titanium tungsten adhesion enhancement layer are deposited in the same vacuum cycle. The sputter deposition of these metals is an established process at the CMST research group and has been executed using the standard parameters without any modifications.
Sputter deposition is preferred over evaporation because of its better step coverage and better adhesion to the substrate. The former is a direct consequence of the relatively large target, i.e. the material source, in case of sputtering, while for evaporation the material can be considered as emerging from a point source. In addition, higher pressures are used for sputtering, resulting in a smaller mean free path of the metal atoms: multiple collisions cause the metal atoms to arrive at the substrate at random incident angles. Sputtering thus generally results in a better coverage of the vias and the edges of the die, guaranteeing continuity of the metallization. Previously, it was suggested that the adhesion of the metallization to the underlying polyimide is improved by exposing its surface briefly to an oxygen (O_2) plasma (Section 3.2.5). However, the roughening step is not performed in this fabrication process due to the small polyimide thickness at the edges of the die. This is illustrated in the cross sections displayed in Figure 4.5.

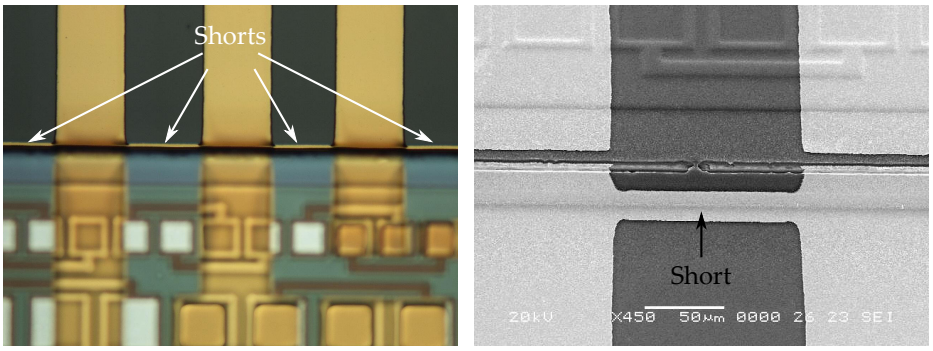
Pattern definition

The metallization is patterned via photolithography and wet etching. In initial experiments, a 1.8 µm thick coating of positive photoresist S1818 was used, which was applied with the standard parameters. However, several problems concerning the quality of the pattern definition were observed. A first problem was already mentioned in Section 4.2.6 where it was shown that the use of a thin layer of photoresist results in a discontinuous coating at the edges of the die (Figure 4.12), causing the titanium tungsten dry etch mask and the PI-2611 film to be etched (Figure 4.14). Similar observations were made for the metallization. This is clearly illustrated in Figure 4.19(a), where the interference fringes indicate that the photoresist gets thinner near the edges of the die and eventually disappears, causing the metallization to be etched at a later stage (also illustrated). The photoresist profile is confirmed by the SEM image in Figure 4.19(b).
Another problem is noticed around the die. Because the die is covered by a 5.5 µm thick PI-2611 film, height variations in the order of the thickness of the die are present which cause photoresist to accumulate around the die during spin coating. If exposure and development times are not optimized to take this into account, the accumulated photoresist is not entirely developed and eventually causes shorts in between adjacent metallic conductors. The shorts are clearly visible in Figure 4.20, but also in the cross section displayed in Figure 4.21.
The above-mentioned problems were both resolved by using a thicker photoresist. To this end, a 6.2 µm thick coating of positive photoresist AZ 4562 is spin



(a) (b)

Figure 4.19: The use of a 1.8 µm thick layer of photoresist S1818 to pattern the metallization results in a discontinuous coating at the edges of the die.



(a) (b)

Figure 4.20: Accumulation of photoresist S1818 around the die causes shorts in between adjacent metallic conductors.

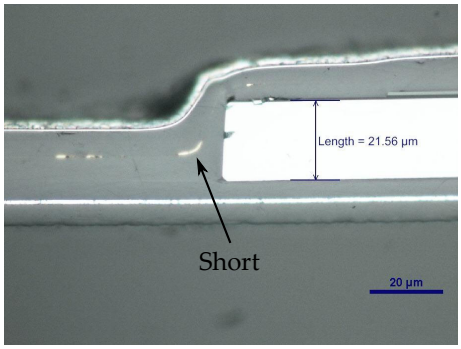


Figure 4.21: Cross section of a 20 µm thick die, at the stage of the fabrication process displayed in Figure 4.1(m), indicating shorts around the die due to accumulation of photoresist S1818 around the die.

coated at 4000 rpm for 60 s, soft baked on a hotplate for 2 min at 90 °C, UV exposed, developed for 1 min in 50 % Microposit^{TM} developer and hard baked for 30 min in a convection oven at 120 °C. The minimum exposure dose required to ensure that no shorts are present was found to depend on the thickness of the die: the photoresist is exposed for 17.5 s and 22.5 s at 10 mW cm^{-2} for die thicknesses of 20 µm and 30 µm, respectively. This is explained by more photoresist accumulating around the die when its thickness increases, thus requiring a larger exposure dose to fully remove the photoresist during development. The optimized photolithography is illustrated in Figure 4.22.

After applying the photoresist, the metallization is wet etched. A solution of iodine (I_2) and potassium iodide (KI) with a mixing ratio of KI : I_2 : DI = 4 g : 1 g : 73 ml is used to pattern the gold. The etching is performed at room temperature and stopped on sight because the etch rate is highly dependent on the mechanical agitation. The underlying titanium tungsten layer is etched in a 30 % H_2O_2 solution at 55 °C for 25 s, followed by a 10 s rinse in a 30 % H_2O_2 solution at room temperature and rinse in deionized water. This process results in well-defined metallization as illustrated in Figure 4.23. In Figure 4.24, also a cross section is shown which illustrates patterned metallization on top of the die.

Important to remark is that the gold etchant has been observed to etch nickel when it is in direct contact with gold. Therefore, attention is required during aligning of the photoresist patterns with respect to the die, both for the pattern definition of the dry etch mask for the second polyimide film POLY2 and for the pattern definition of the metallization. An aligning error in the former case can result in side surfaces of the nickel portion of the ENIG surface finish which are not shielded from the gold etchant, while an aligning error in the latter case results in an unshielded upper surface of the ENIG surface finish. These situations

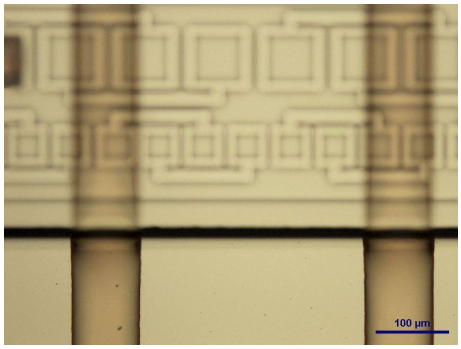


Figure 4.22: Optimized photolithography based on AZ 4562 for the pattern definition of the metallization for a 20 µm thick die.

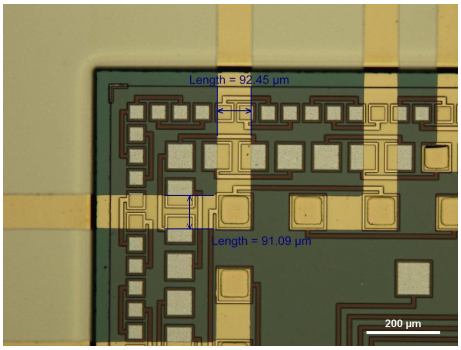
led to detachment and / or etching of the ENIG surface finish (Figure 4.25).

4.2.9 Structuring of PI-2611

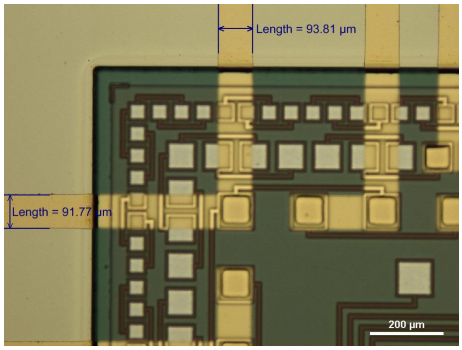
After covering the patterned metallization with another layer of PI-2611 (POLY3; Figure 4.1(m)), the different polyimide films (POLY1, POLY2 and POLY3) are structured to achieve polyimide covered meandering conductors and polyimide islands hosting the thin die, footprints (e.g. for SMD components), etc. This is done by dry etching, as patterning PI-2611 films using traditional wet etch techniques is difficult because of its chemical inertness.

Masking layer

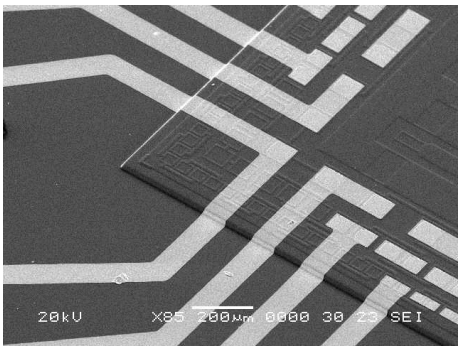
An etch mask is required to pattern the PI-2611 films by dry etching. To this end, a 20 nm thick titanium tungsten adhesion enhancement layer and a 200 nm thick aluminium film are sputter deposited in the same vacuum cycle. Aluminium is the preferred hard mask since it is inert for the oxygen (O_2) and trifluoromethane (CHF_3) chemistry used to etch PI-2611.
Both metal films are patterned via photolithography and wet etching. To this end, a 6.2 µm thick coating of positive photoresist AZ 4562 is spin coated at 4000 rpm for 60 s, soft baked on a hotplate for 2 min at 90 °C, UV exposed for 17.5 s at 10 mW cm^{-2}, developed for 1 min in 50 % Microposit^{TM} developer and hard baked for 30 min in a convection oven at 120 °C. Note that the aluminium mask has to be aligned relative to the gold patterns. Height variations in the covering polyimide film POLY3 caused by the underlying gold patterns facilitate the aligning and exclude an additional processing step for exposing the alignment marks.



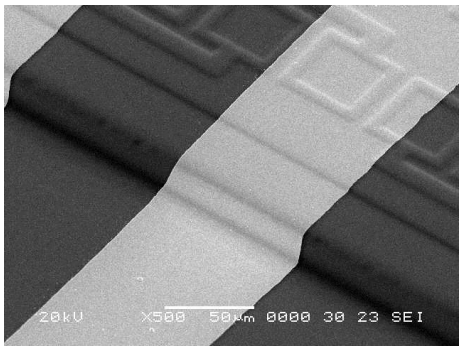
(a) 20 µm thick die.



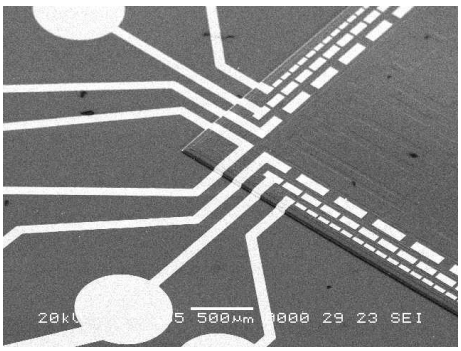
(b) 20 µm thick die.



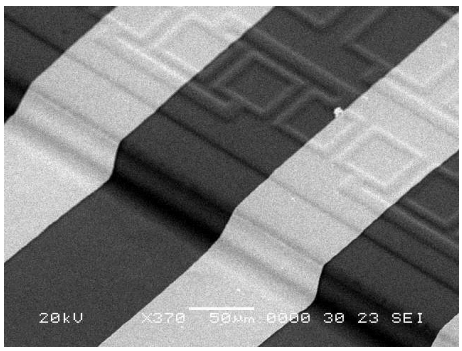
(c) 20 µm thick die.



(d) 20 µm thick die.



(e) 30 µm thick die.



(f) 30 µm thick die.

Figure 4.23: Well-defined metallization at the edges of 20 µm and 30 µm thick dies.

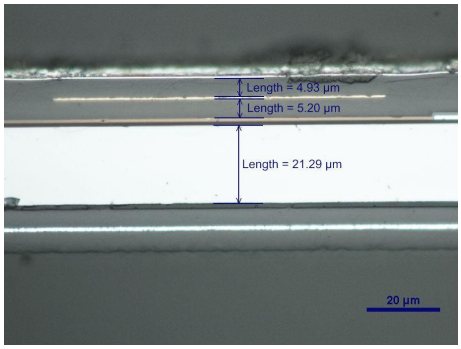
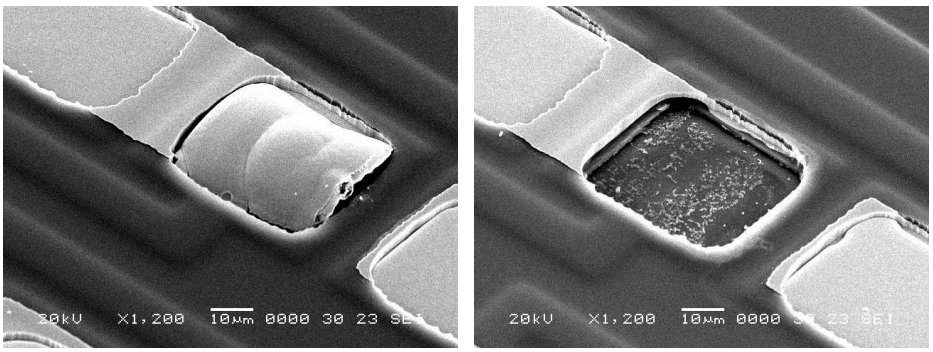


Figure 4.24: Cross section of a 20 µm thick die, at the stage of the fabrication process displayed in Figure 4.1(m), illustrating patterned metallization on top of the die.



(a) (b)

Figure 4.25: Detachment and / or etching of the ENIG surface finish due to bad aligning of the photoresist patterns with respect to the die.

Step #	Description	Parameters
(a)	Sputter deposit TiW	Thickness: 50 nm,
	(Alcatel SCM600)	DC power: 1200 W
		Chamber pressure: 1×10^{-2} mbar
	Sputter deposit Au	Thickness: 200 nm,
	(Alcatel SCM600)	DC power: 1000 W,
		Chamber pressure: 1×10^{-2} mbar
(b)	Spin coat AZ 4562	60 s at 4000 rpm
	Soft bake	Hotplate, 2 min at 90 °C
	UV exposure	17.5 s or 22.5 s at 10 mW cm^{-2}
	Development	50 % Microposit^{TM} developer, 1 min
	Hard bake	Convection oven, 30 min at 120 °C
(c)	Wet etch Au	Au etchant (see text), on sight
	DI rinse	2 min
	Wet etch TiW	30 % H_2O_2, 25 s at 55 °C
		30 % H_2O_2, 10 s at RT
	DI rinse	2 min

Table 4.6: Process parameters for the metallization.

After application of the photoresist, the hard mask is wet etched. A solution of acetic acid (CH_3COOH, > 99 %), nitric acid (HNO_3, > 65 %) and phosphoric acid (H_3PO_4, > 89 %) with a mixing ratio of CH_3COOH : HNO_3 : H_3PO_4 : DI = 4 : 1 : 4 : 1 is used to pattern the aluminium film. The etching is performed at room temperature, without mechanical agitation. The etch rate is approximately 20 nm min^{-1}. Substrates are thoroughly rinsed in deionized water after etching to remove any residual acid. The underlying titanium tungsten layer is etched in a 30 % H_2O_2 solution at 55 °C for 15 s, followed by a 10 s rinse in a 30 % H_2O_2 solution at room temperature and rinse in deionized water.
After dry etching, the hard mask is completely removed using an identical wet etch procedure. Both the hard mask and the aluminium film which is part of the release stack are exposed to the etchants. Because the latter has a thickness of 1 µm, the 200 nm thick hard mask can be removed without completely sacrificing the latter. Remember that the aluminium film which is part of the release stack is required to avoid contamination of the etch tool (refer to the paragraph on volatility of PDMS in Section 2.4.3).

Dry etching

The different polyimide films (POLY1, POLY2 and POLY3), which have a total thickness of 16.5 µm, are etched using the optimized dry etch parameters de-

scribed in Section 3.2.6. For the design displayed in Figure 4.31, the etch time was found to be 70 min. A surface scan of the etched stack, taken using an optical profiler WYKO NT3300 (Veeco), is displayed in Figure 4.26(a). As noticed in Figure 4.26(b) and Figure 4.26(c), the PI-2611 stack is successfully structured and has a thickness of approximately 16.5 µm.

It was also verified that the gold film, like the aluminium film, effectively serves as a masking layer for the dry etching. This allows providing contact pads to the gold conductors by etching the top polyimide film POLY3, as schematically illustrated in Figure 4.1(p) and illustrated for the circular probing pads in Figure 4.27.

4.2.10 Placement of components

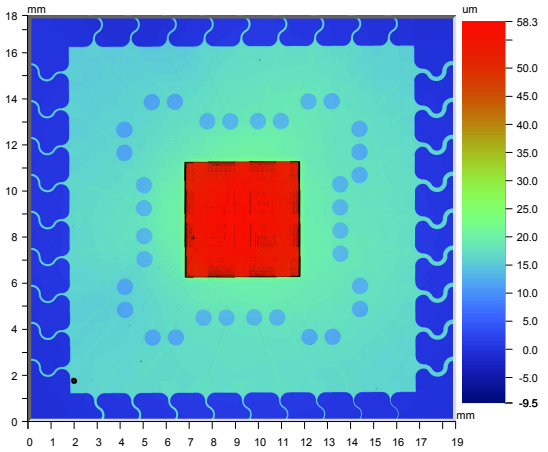
Although this is not required for the test design for the PTCE silicon dies, conventional off-the-shelf components (e.g. SMD) can be mounted on exposed gold metallization. This is done by means of anisotropic or isotropic conductive adhesives, as explained in Section 3.2.7.

4.2.11 Encapsulation in PDMS

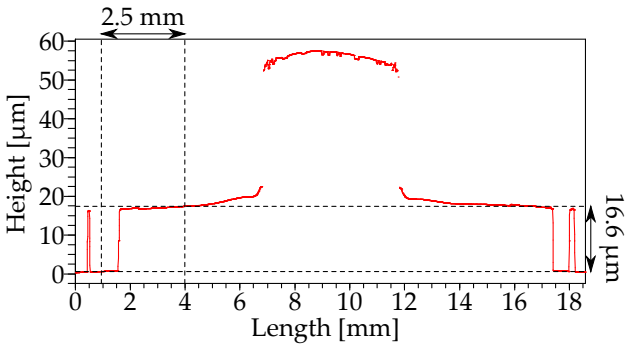
Encapsulation in PDMS can be done either by spin coating or liquid injection molding, both in two phases to provide full encapsulation. The former method is chosen when thin, uniform films of PDMS are desired, while for the latter method the substrate is clamped in between two machined PMMA molds, offering the possibility of performing non-uniform 3-D encapsulation. For the PTCE silicon dies, the PDMS is spin coated.

Two types of PDMS are used: Silastic® MDX4-4210 and MED-6010. Prior to application of the first (but also the second) layer of PDMS, 1200 OS Primer is applied to the substrate for improved adhesion of the PDMS to the polyimide structures. To this end, the substrate surface is cleaned using a wipe with IPA. Next, a thin film (!) of the primer is applied using a clean wipe. As the primer is usually activated by atmospheric moisture, it is allowed to air dry for 15 min before applying the PDMS. If a white chalky residue is noticed, the residue is removed by means of a clean wipe.

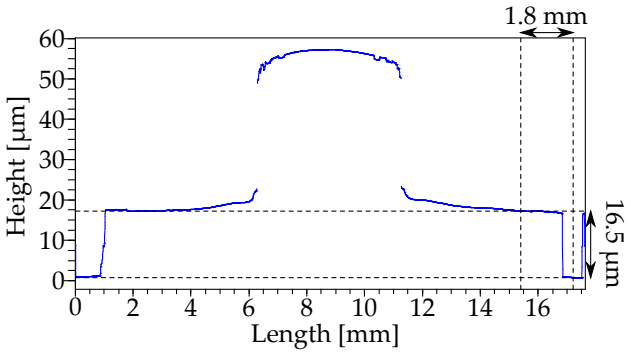
After applying the first layer of PDMS, it is cured for 4 h in ambient atmosphere in a convection oven at 50 °C (Figure 4.1(r)). The stack is then released from the rigid carrier and the sacrificial layers are removed according to the procedure described in Section 3.2.3. Subsequently, the encapsulation procedure is repeated at the bottom side of the released membrane. The encapsulated test design is shown in Figure 4.28.



(a) Overview.



(b) Cross-sectional profile along the horizontal centerline.



(c) Cross-sectional profile along the vertical centerline.

Figure 4.26: Surface scan of the structured PI-2611 stack.

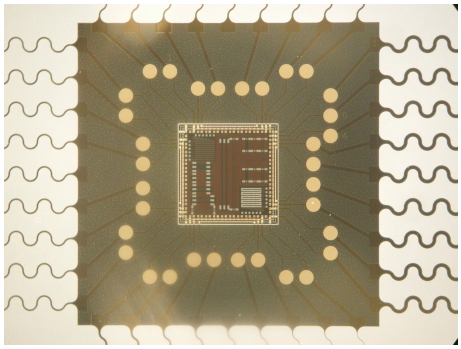
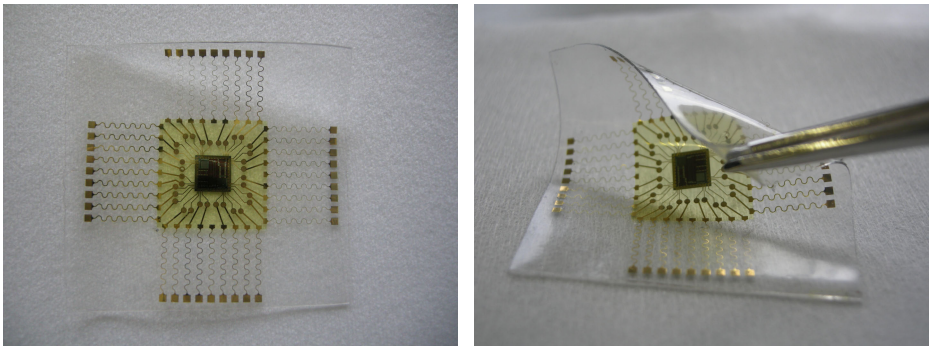


Figure 4.27: Stretchable circuit on the release stack after patterning the entire PI-2611 stack.



(a) (b)

Figure 4.28: Stretchable circuit with thin PTCE die, encapsulated in a 240 µm thick membrane of Silastic® MDX4-4210.

Step #	Description	Parameters
(a)	Sputter deposit TiW	Thickness: 20 nm,
	(Leybold Z550)	DC power: 1200 W,
		Chamber pressure: 1×10^{-2} mbar
	Sputter deposit Al	Thickness: 200 nm,
	(Leybold Z550)	DC power: 2000 W,
		Chamber pressure: 2×10^{-3} mbar
(b)	Spin coat AZ 4562	60 s at 4000 rpm
	Soft bake	Hotplate, 2 min at 90 °C
	UV exposure	17.5 s at 10 mW cm^{-2}
	Development	50 % Microposit^{TM} developer, 1 min
	Hard bake	Convection oven, 30 min at 120 °C
(c)	Wet etch Al	Al etchant (see text), 10 min
	DI rinse	2 min
	Wet etch TiW	30 % H_2O_2, 15 s at 55 °C
		30 % H_2O_2, 10 s at RT
	DI rinse	2 min
(d)	Strip AZ 4562	Acetone, 2 min
	IPA rinse	2 min
	DI rinse	2 min
(e)	Dry etch PI-2611	70 min (see text)
	(System VII Batchtop RIE)	RF power: 150 W,
		Chamber pressure: 150 mTorr,
		O_2 flow rate: 15 sccm,
		CHF_3 flow rate: 5 sccm
(f)	Wet etch Al	Al etchant (see text), 10 min
	DI rinse	2 min
	Wet etch TiW	30 % H_2O_2, 90 s at 55 °C
		30 % H_2O_2, 10 s at RT
	DI rinse	2 min

Table 4.7: Process parameters for the structuring of PI-2611.

	Size [µm]	Pitch [µm]	Number of pads
Inner row	90	200	84
Middle row	70	100	180
Outer row	40	60	316

Table 4.8: Size, pitch and number of square pads for the different daisy chain test structures on the PTCE die.

4.3 Evaluation

So-called daisy chain silicon dies (Section 4.3.1) were chosen to illustrate the capabilities of the presented fabrication technology. The die and the corresponding mask design allow for quantification of the contacting yield from the package to the die level, through both single via and daisy chain resistance measurements (Section 4.3.2).

4.3.1 PTCE silicon die

Description

The platform described in this chapter is developed with PTCE ("Packaging Test Chip version E") silicon dies, designed and provided by imec. The dies were thinned down on wafer scale at DISCO HI-TEC EUROPE GmbH from an initial thickness of 725 µm, which is the standard thickness of an 8 inch silicon wafer, to a final thickness of either 20 µm or 30 µm. To this end, a dicing before grinding (DBG) methodology (Section 2.2.3) was used. The wafer is half-cut from the circuit side with a special dicing saw, backgrinding tape is affixed and backgrinding is performed. After obtaining the desired thickness, the grooves formed by half-cut dicing are reached and singulated dies are obtained.
A microscope picture of a 30 µm thick PTCE die is shown in Figure 4.29 and illustrates the layout. The die measures 5 mm by 5 mm. Several devices such as daisy chain, triple track and high frequency test structures are implemented on the die, and are composed of 1 µm thick aluminium metallization passivated with silicon nitride. However, only the daisy chain test structures at the periphery of the die are used in this work. These are displayed in Figure 4.30. The different interconnection schemes are indicated by distinct colors, while enlarged views are displayed at the right. Three types of daisy chain test structures are present. The pitch and size (between brackets) of the square pads are 200 µm (90 µm), 100 µm (70 µm) and 60 µm (40 µm), moving from the inner row to the outer row. The details on the pad layout are also summarized in Table 4.8.

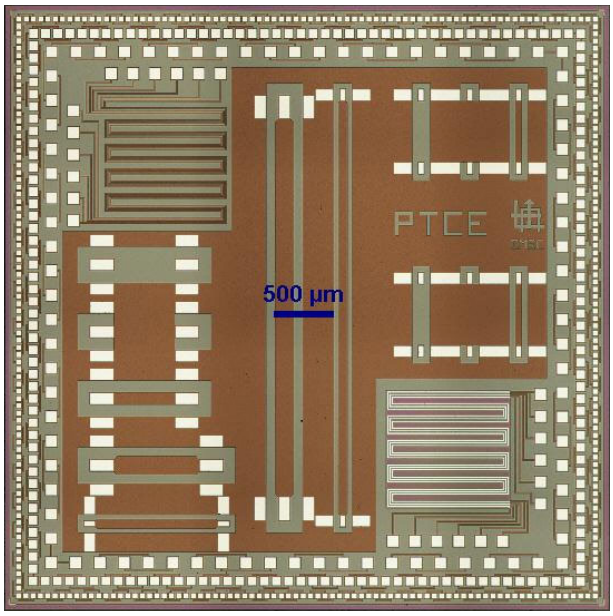


Figure 4.29: Microscope picture of a 30 µm thick PTCE die.

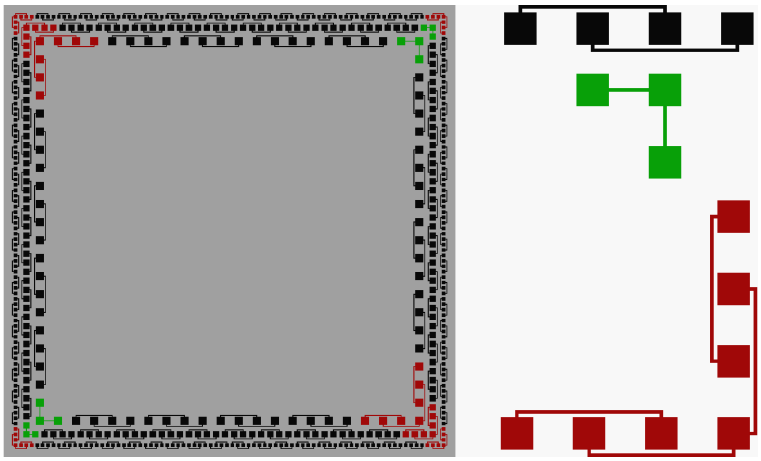
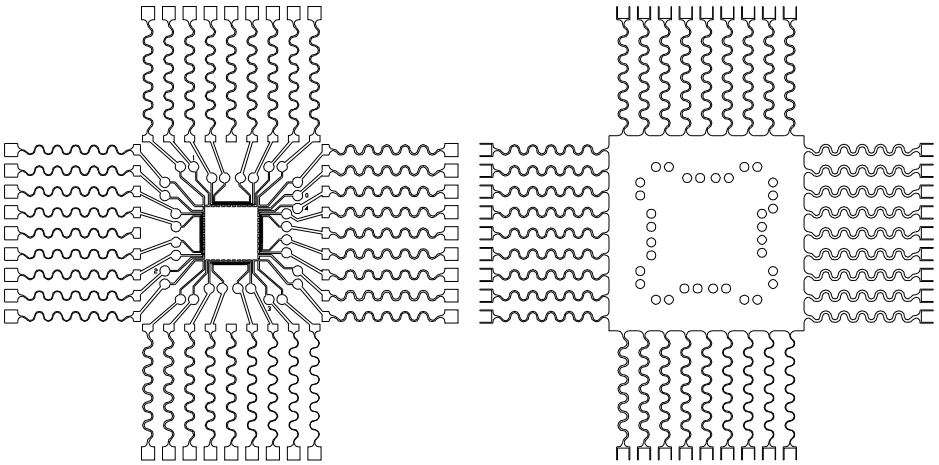


Figure 4.30: Schematic representation of the PTCE die displaying only the daisy chain test structures at its periphery. The different interconnection schemes are indicated by distinct colors, while enlarged views are displayed at the right.



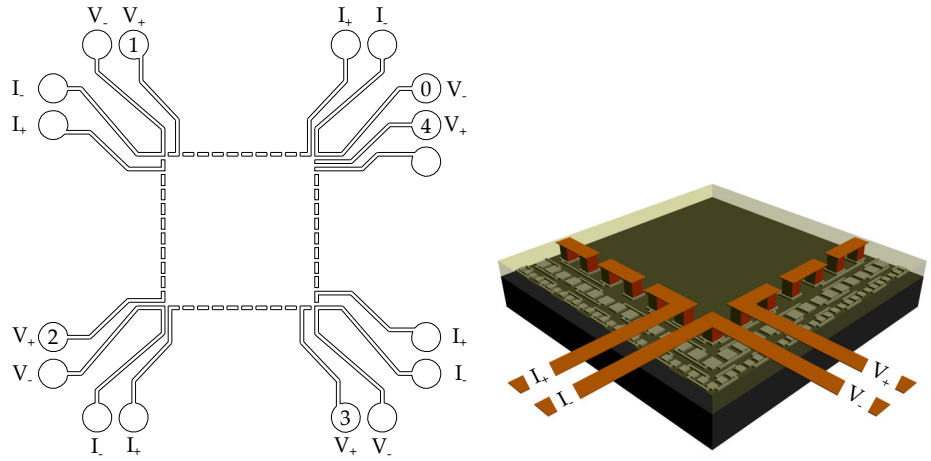
(a) Metallization. (b) Polyimide.

Figure 4.31: Mask design at the package level for the PTCE dies.

The different daisy chain test structures on the PTCE die provide a wiring scheme so that multiple vias can be connected in series if a proper design for the metallization at the package level is introduced: 80, 176 and 312 vias respectively when moving from the pads with the coarsest pitch to the pads with the finest pitch. The series connection of the vias allows for quantification of the contacting yield from the package to the die level.

Test design

The mask design at the package level for the PTCE dies is shown in Figure 4.31. The PTCE die is embedded in a polyimide island at the center of the design. The meandering horseshoe shaped interconnections surrounding the polyimide island are introduced to illustrate the stretchability, but do not allow testing of the mechanical performance. The fan-out metallization towards the 0.7 mm circular probing pads allows for electrical characterization of the daisy chain test structures. Although probing pads are foreseen for the three types of daisy chain test structures, only the inner row is used for measurements. The vias for the inner row are designed identically as squares with a side length of 75 µm.
A zoomed view of the metallization at the package level for the inner row of pads is shown in Figure 4.32(a). In between two adjacent tagged circular pads (‘0’, ‘1’, ‘2’, ‘3’ and ‘4’), a series connection of 20 vias is present. The design also allows for resistance measurement of single vias at the corners of the die through 4-point probe methodology: current is sourced through the circular pads tagged with the



(a) Zoomed view. (b) 3-D impression.

Figure 4.32: Metallization at the package level for the inner daisy chain test structures of the PTCE dies.

symbols 'I_+' and 'I_-' while the corresponding voltage drop is measured over the circular pads tagged with the symbols 'V_+' and 'V_-'. A 3-D impression of part of the daisy chain series at the corner of the die is given in Figure 4.32(b) and illustrates the metallization on a packaged PTCE die.

4.3.2 Electrical performance

Test setup

A source measure unit (SMU; Keithley 236) was used to source current through the series connections of vias and simultaneously measure the corresponding voltage drop. This was done by connecting the SMU via a probe station to the 0.7 mm diameter circular probing pads, displayed in Figure 4.32(a). For practical reasons, the electrical measurements were performed before encapsulation in PDMS while the package was still supported by the glass substrate (Figure 4.1(q)). This way, the circular probing pads were minimally damaged, and patterning of the top PDMS layer (PDMS1) is avoided.

Single via resistance

As shown in Figure 4.32(a), the test design allows single via resistance measurements to be performed at each corner of the die. A distinction is made between two sets of single via resistance measurements corresponding to the different cor-

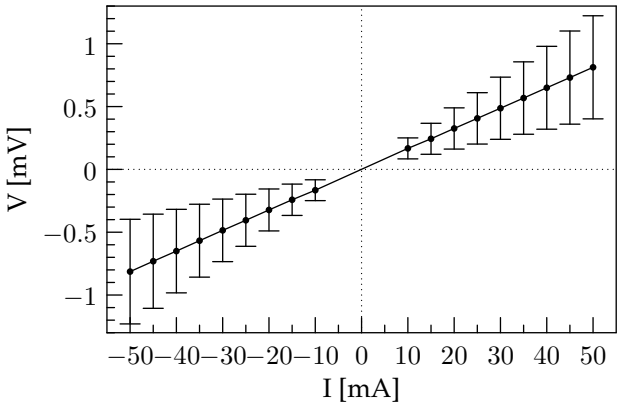
ner lay-outs of the die (Figure 4.30). Set 1 corresponds to the measurements performed at the top right and bottom left corner, while set 2 corresponds to the measurements performed at the top left and bottom right corner displayed in Figure 4.30. To determine the resistance, different currents were sourced ranging from 10 mA to 50 mA (step size = 5 mA), and the corresponding voltage drop was measured. Because an offset voltage is generally present during these measurements, currents were sourced in both directions to allow cancellation of the offset.
The results of single via resistance measurements performed on 14 packaged dies are graphically represented in Figure 4.33; each voltage drop represents the average of 28 measurements. A linear relationship between the current and the voltage drop is observed, indicating a well-defined ohmic resistance. Using these values, the single via resistance of set 1 and set 2 is calculated to be R_1 = 16.3 mΩ ± 8.14 mΩ and R_2 = 7.43 mΩ ± 3.24 mΩ, respectively. The difference in resistance value for both sets of vias is explained by the varying design of the on-chip metallization (Figure 4.30).

Daisy chain resistance

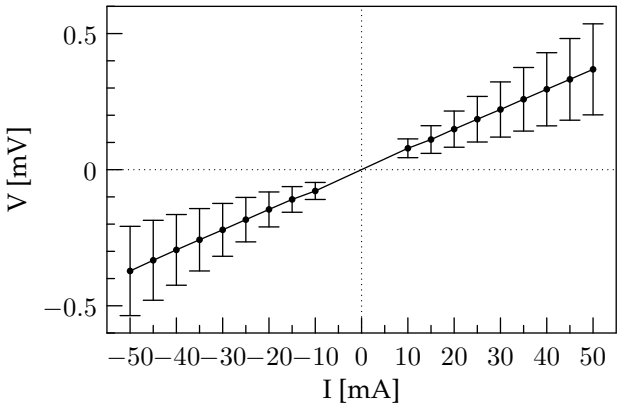
Four sets of daisy chains consisting of 20, 40, 60 and 80 vias were studied by sourcing currents ranging from 10 mA to 50 mA (step size = 5 mA). As with the single via resistance measurements, also the reversed current was sourced to allow cancellation of the offset.
Measurements were performed on a total number of 14 packaged dies. It was found that two out of a total number of 1120 vias suffered from bad contacts, indicating a via yield of 99.82 %. The resistance of each set of daisy chain was determined as R_a = 27.2 Ω ± 0.624 Ω, R_b = 46.1 Ω ± 1.06 Ω, R_c = 62.9 Ω ± 1.43 Ω and R_a = 81.2 Ω ± 1.89 Ω. The vias thus have a limited contribution to the resistance of the daisy chains which is mainly determined by the resistance of the thin metallization on the die and package level, 1 µm thick aluminium and 200 nm thick gold, respectively.

4.4 Conclusions

A technology platform enabling conformable, stretchable electronic systems has been developed. It is based on the pixelated architecture described in Chapter 2: islands of a structural, non-stretchable material host active electronic components or subcircuits and are connected through the stretchable electrical wiring presented in Chapter 3. Whereas in related approaches electronic components are assembled on the non-stretchable islands in conventional ways or require custom microfabrication, in this chapter focus has been put on the implementation of electronic components by embedding them as thin dies in a slim polyimide package. This methodology avoids the use of conventional bulky packaged dies



(a) Set 1.



(b) Set 2.

Figure 4.33: Single via resistance measurements performed on packaged PTCE dies. The error bars represent the standard deviation s of the voltage drops consisting of 28 measurements.

(e.g. SMD), and as such improves the miniaturization and the conformability of the electronic systems.
Unpackaged silicon dies were thinned from their original thickness to thicknesses of 20 µm - 30 µm, and embedded in between several spin-on polyimide films. The fan-out metallization is configured as polyimide-supported horseshoe shaped gold conductors. By subsequent encapsulation in a silicone elastomer, i.e. PDMS, a system is achieved that can stretch and flex, the latter even at the location of the non-stretchable islands. The fabrication process was designed to enable simultaneous fabrication of the stretchable electrical interconnections and packaging of the thinned dies. Furthermore, care was taken to use solely processing steps which are compatible with thin-film processing.
The technology was demonstrated by thinning and embedding so-called daisy chain silicon dies. This die and its corresponding mask design allows for quantification of the contacting yield from the package to the die level, through both single via resistance and daisy chain resistance measurements. Single via resistances as low as a couple of mΩ have been measured, while the daisy chain resistance measurements highlighted the reliable character of the technology by a via yield of 99.82 %.

References

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5
PDMS-based Microfluidics

5.1 Introduction

In its early stages, microfluidics benefited greatly from microfabrication technologies developed for semiconductors by the microelectronics industry: photolithography and etching techniques developed for silicon and glass were used to fabricate the first microfluidic devices, as these techniques were available, well established and precise. However, the production of silicon or glass microfluidic devices is generally expensive and time-consuming, and requires access to cleanroom facilities. Consequently, their use in research requiring rapid evaluation of prototypes is limited, and there has been a gradual shift towards alternative, cheaper materials and techniques. The focus hence shifted towards polymers such as poly(methyl methacrylate) (PMMA), polycarbonate, polyimide, SU-8 or PDMS, and techniques such as laser ablation, hot embossing, injection molding or replica molding.

Although various polymers have become popular in the field of microfluidics, PDMS in particular is of interest as it really has boosted research due to its low cost and ease of use. Soft-lithographic techniques are used to replicate the relief structures present on the surface of a mold; these techniques allow for rapid prototyping, do not require cleanroom facilities and benefit greatly from the flexibility of PDMS.

In the first section of this chapter, the fabrication process for PDMS-based microfluidics consisting of a single fluidic layer is described. To this end, master molds are fabricated using SU-8 photolithography, which are then used to

micropattern PDMS via replica molding. The next section introduces an aligning and bonding methodology for multiple micropatterned PDMS layers, and is subsequently used for the integration of membranes in between multiple fluidic layers. In the last section, a methodology is described to add electronics (e.g. sensors) to the microfluidic devices. Particular attention is spent to combine the PDMS-based microfluidics with the technology presented in Chapter 4.

5.2 Fabrication process

The fabrication process for PDMS-based microfluidics consisting of a single fluidic layer is described in detail. In the next section, Section 5.3, multi-layered microfluidics will be discussed.

5.2.1 Overview

A schematic representation of the fabrication process for PDMS-based microfluidics is shown in Figure 5.1. Each step will be discussed in detail in the following, corresponding sections. First, a master mold (Section 2.3.2) is fabricated via SU-8 photolithography (Figure 5.1(a) - Figure 5.1(d)). Next, the surface of a PDMS membrane is patterned by replicating the three-dimensional topography of the master mold. This is done by a sequence of casting, curing and peeling (Figure 5.1(e) - Figure 5.1(g)). Enclosed channels are subsequently obtained by conformal contact of activated surfaces (Figure 5.1(h) - Figure 5.1(j)).

5.2.2 Fabrication of the master mold

Master molds can be fabricated in several ways: photoresist films can be deposited and patterned on various substrates, polymer films or substrates can be wet or dry etched, etc. The most popular method, however, uses patterned films of SU-8 as this technique only requires photolithography, thus avoiding critical etching steps, and allows for feature sizes which are typical for microfluidics.

Introduction to SU-8

SU-8 is a high-contrast, negative tone, epoxy based photoresist developed by MicroChem. It is designed for micromachining and microelectronic applications, requiring thick, high-aspect ratio chemically and thermally stable polymer features. The film thickness achieved during a conventional single spin coat process depends on the SU-8 viscosity, and ranges from $< 1\,\mu m$ for the least viscous to $> 200\,\mu m$ for the most viscous formulation. Using multiple coatings or adapted coating techniques, film thicknesses as high as 1.5 mm have been achieved [1]. It has to be noted that SU-8 is best suited for permanent applications where it

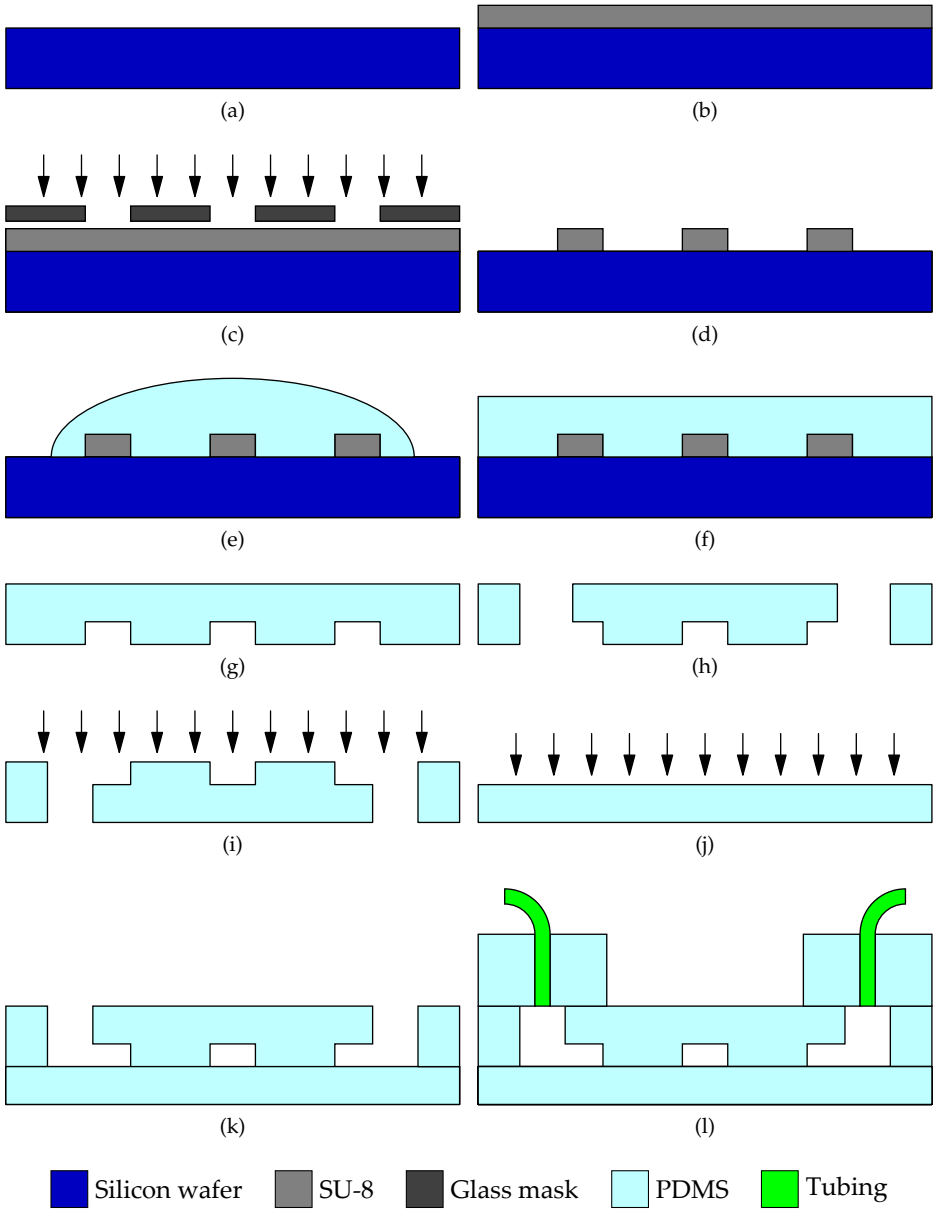


Figure 5.1: Fabrication process for PDMS-based microfluidics: cross-sectional views of the fabrication steps (not drawn to scale; a brief description is found in Section 5.2.1).

is imaged, cured and left in place, as is the case with the master molds (Figure 5.1(d)).
During the course of this research, MicroChem developed two new, improved series of SU-8. Aside from the standard SU-8 series, which suffers from relatively high internal stresses and bad adhesive properties, also the SU-8 2000 and SU-8 3000 series became available. The SU-8 2000 series uses a faster drying, more polar solvent system, resulting in improved coating quality and increased process throughput (e.g. by shorter baking steps). It was observed that the SU-8 2000 series had an improved adhesion to the substrate, but it was also noticed that they are quite susceptible to air bubbles. Although there are some tricks such as heating the bottle in an upright position before spin coating, as this reduces the viscosity and allows the air bubbles to rise out of the photoresist, it was very difficult to achieve bubble free coatings with the SU-8 2000 series. The SU-8 3000 series, the latest formulation, is less susceptible to air bubbles, and allows for improved adhesion and reduced coating stress. The process described in what follows, is based on SU-8 photoresists from the SU-8 3000 series.

Substrate

The substrate is part of the master mold (as indicated in Figure 5.1(d)), which is preferably reusable. The SU-8 features thus have to adhere well to the substrate [2]. As the surface topography is replicated in PDMS by a sequence of casting, curing and peeling, the substrate also has to allow for an easy separation of the PDMS.
Silicon wafers are chosen as substrate, as these were experimentally found to comply with above-mentioned requirements, but also eased process optimization as the process parameters mentioned in the SU-8 product data sheet are valid for silicon substrates. In this work, silicon wafers with a diameter of 4 inch (10.16 cm) were used, and had a thickness of 525 µm.
Prior to processing, the silicon wafers are thoroughly cleaned to remove organic residues, followed by a dehydration bake on a hotplate. The dehydration bake was found necessary in order to ensure a good adhesion of the SU-8 features. The cleaning procedure normally comprises an acetone, acetone / isopropyl alcohol and deionized water soak sequence, and is summarized in Table 5.1.

SU-8 photolithography

After the dehydration bake, the silicon wafer is allowed to cool to room temperature and a layer of SU-8 is spin coated. Photoresists from the SU-8 3000 series are available in five standard viscosities. The target thickness determines which viscosity is most suited; this can be derived from the spin speed curves shown in Figure 5.2 [3].
As it was observed that pipetting introduces numerous air bubbles in the deposited material, SU-8 is poured directly from the bottle onto the wafer. There-

Step #	Description	Parameters
(a)	Rinse in a beaker with acetone	5 min
	Rinse in a beaker with acetone / IPA	5 min
	Rinse in a beaker with DI	2 min
	Rinse with DI pistol	
(b)	Dehydration bake	Hotplate, 30 min at 250 °C

Table 5.1: Cleaning procedure for the silicon wafers.

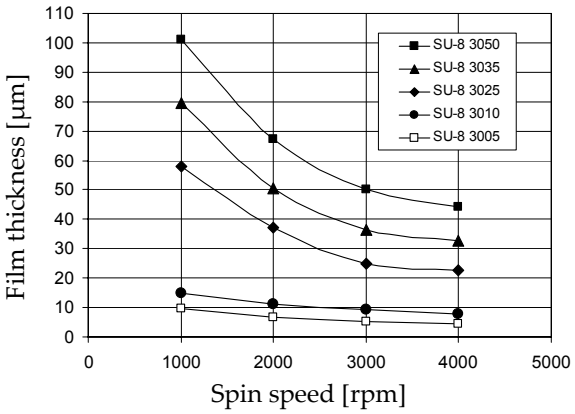


Figure 5.2: Spin speed curves for the different photoresists from the SU-8 3000 series, coated for 30 s at the indicated speed [3].

fore, in order for the process to be reproducible, the original bottle of SU-8 is distributed over multiple smaller bottles upon its first use. Approximately 4 ml is deposited at the center of the silicon wafer. Spin coating is performed in two stages: an intermediate spin speed of 500 rpm is used to gradually cover the wafer before continuing to the final spin speed. The final spin speed and spin time determine the thickness of the coating, and can be deducted from the spin speed curve in Figure 5.2. Slight deviations of these values are however possible, e.g. a coating thickness of 50 µm is achieved with a final spin speed of 2700 rpm for 30 s.

After spin coating (Figure 5.1(b)), the edge bead is removed as this would increase the distance between the glass mask and the wafer during exposure. This is particularly necessary for thick coatings for clear reasons, and is performed manually by scraping the outer edge of the coated wafer with a clean dummy glass substrate. The coating is then soft baked on a hotplate. A temperature profile with dwell temperatures of 65 °C and 95 °C, and intermediate ramping is used to allow gradual evaporation of solvents and to reduce thermal stresses.

Next, parts of the SU-8 coating are cross-linked. The coating is exposed to UV radiation through a glass mask (Figure 5.1(c)), introducing a strong acid in the exposed regions; i-line (365 nm) is recommended. It has been reported that wavelengths shorter than 350 nm are strongly absorbed near the top surface, causing lateral diffusion of the acid and resulting in so-called T-topping [4, 5]. Therefore, in order to obtain vertical sidewalls, a long pass filter PL-360-LP (Omega Optical) is used to eliminate UV radiation below 350 nm. Using such a filter increases the exposure time by approximately 40 % to achieve the optimum exposure dose.

The acid induced during UV exposure subsequently acts as a catalyst for the thermally driven cross-linking during the post exposure bake. As is the case with the soft bake, the post exposure bake occurs in two steps at 65 °C and 95 °C to avoid temperature shocks. After allowing the wafer to cool to room temperature, the unexposed regions are removed with MicroChem's SU-8 developer (Figure 5.1(d)). Development times are indicative as these are strongly dependent on the agitation. The development is followed by a rinse in isopropyl alcohol. Optionally, a hard bake can be introduced after developing to further cross-link the SU-8.

As an example, the process parameters for 50 µm thick SU-8 3050 features are summarized in Table 5.2. The thickness uniformity was characterized using an optical profiler WYKO NT3300 (Veeco). The thickness of the SU-8 features was measured at five well-distributed spots along the outline of a cross, one spot at the centre of the substrate and four spots at approximately 1 cm from each of the substrate edges, and an average was calculated. The corresponding results are mentioned in Table 5.3 for five different master molds.

Step #	Description	Parameters
(a)	Manual, static dispense	Approximately 4 ml
(b)	Spin coat	Start at 500 rpm, Hold 10 s at 500 rpm, Ramp to 2700 rpm at 500 rpm s^{-1}, Hold 30 s at 2700 rpm
(c)	Edge bead removal	Manually with dummy substrate
(d)	Soft bake	Hotplate, 3 min at 65 °C, Ramp to 95 °C, 15 min at 95 °C
(e)	UV exposure	PL-360-LP filter, 35 s at 10 mW cm^{-2}
(f)	Post exposure bake	Hotplate, 1 min at 65 °C, no ramp, 5 min at 95 °C
(g)	Development	SU-8 developer (old), 2.5 min, SU-8 developer (fresh), 30 s,
	IPA rinse	1 min
(h)	Hard bake	Convection oven, ramp to 120 °C, 90 min at 120 °C

Table 5.2: Process parameters for 50 µm thick SU-8 3050 features.

Sample #	Average thickness [µm]	Std. dev. [µm]
1	55.5	4.2
2	49.5	2.4
3	51.4	1.0
4	51.5	1.7
5	47.4	1.8

Table 5.3: Characterization of the thickness uniformity of SU-8 3050 features.

5.2.3 Micropatterning of PDMS

The surface of a PDMS membrane is micropatterned by replicating the three-dimensional topography of a master mold. This is done by a sequence of casting, curing and peeling. The PDMS is prepared and degassed according to the procedure described in Section 2.4.3. It is then applied on the master mold in its liquid state (Figure 5.1(e)) and cured (Figure 5.1(f)). As cross-linking is initiated directly after mixing, gradually increasing the viscosity of the liquid prepolymer, the time that elapses between degassing and application onto the master mold is minimized. The latter can be as simple as pouring a certain volume of liquid prepolymer onto the master mold, but also more advanced techniques such as spin coating or embossing can be used if a specific membrane thickness is targeted.
The embossing process is schematically represented in Figure 5.3. The stack consisting of the master mold and the liquid prepolymer is placed in between the two plates of a hydraulic Carver press 12-12H which are used to apply controlled pressure on the stack. Optionally, the plates provide heating, allowing the cross-linking of PDMS while exerting pressure. Embossing offers the advantage that a temporary carrier for the patterned PDMS membrane is easily introduced. The temporary carrier is carefully placed on top of the liquid prepolymer so as to avoid trapping air bubbles, and is preferably a flexible material (e.g. PET or polyimide foils) to allow easy separation of the stack from the master mold. This is of specific interest for (very) thin membranes, as the temporary carrier eases the peeling from the master mold and the handling.
Cure conditions vary for the different types of PDMS or in function of specific requirements. Curing can be performed at elevated temperatures if rapid prototyping is desired, or at room temperature for several days if a minimal shrinkage of the PDMS (CTE ranging from $300\,\mathrm{ppm}\,^{\circ}\mathrm{C}^{-1}$ to $400\,\mathrm{ppm}\,^{\circ}\mathrm{C}^{-1}$) is desired. In a final stage, the cured PDMS membrane is peeled from the master mold and a negative replica is obtained (Figure 5.1(g)). Micropatterned surfaces of Sylgard® 184 and Silastic® MDX4-4210, with feature heights of $50\,\mu\mathrm{m}$, are illustrated in Figure 5.4.

5.2.4 Bonding of PDMS

Native, cross-linked polydimethylsiloxanes exhibit low surface energies. Contact angle measurements illustrate the hydrophobic nature; these were experimentally measured to be in the range of 120° for the different types of PDMS used during this research (Figure 5.5). However, it is known that the surface properties of cross-linked PDMS can be altered by exposure to various energy sources such as air or oxygen plasmas, ultra violet light or corona discharges [6–10]. The reactions which occur are complex, though it is believed that upon exposure silanol groups (Si-OH) are generated on the PDMS surface at the expense of methyl groups (Si-CH_3) [6, 7, 11]. To achieve enclosed microchannels, the activated surface of the patterned PDMS membrane is brought into conformal contact with a second sur-

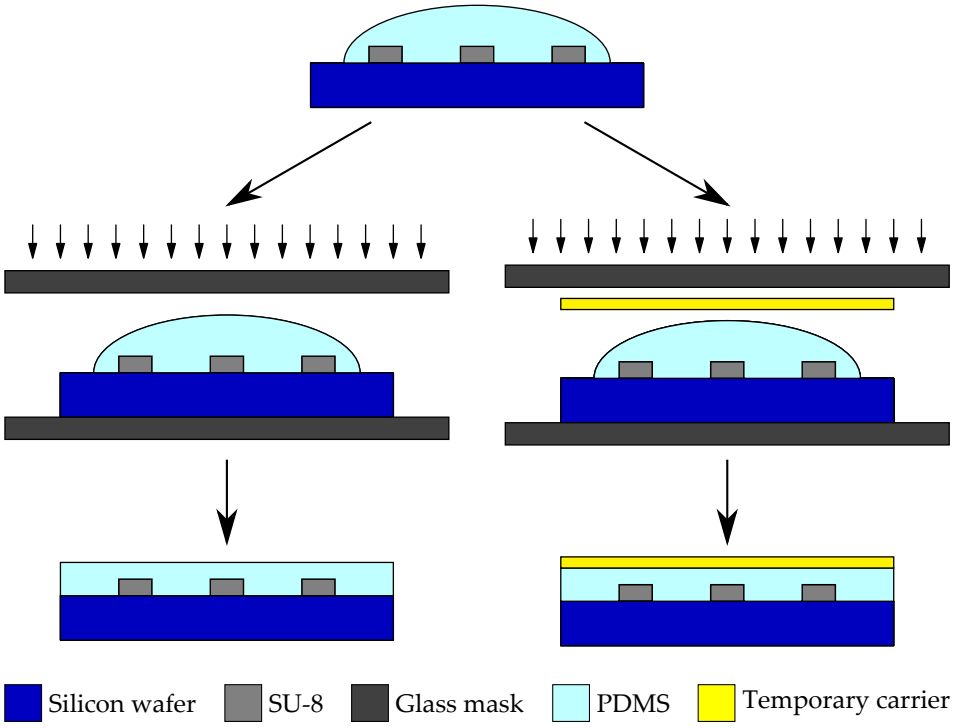
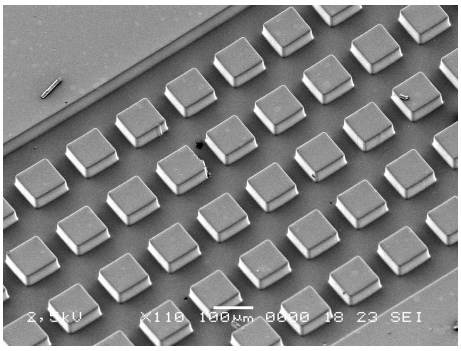
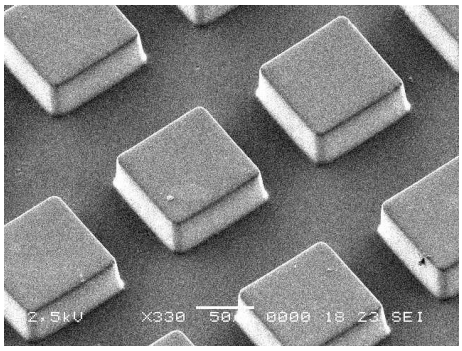


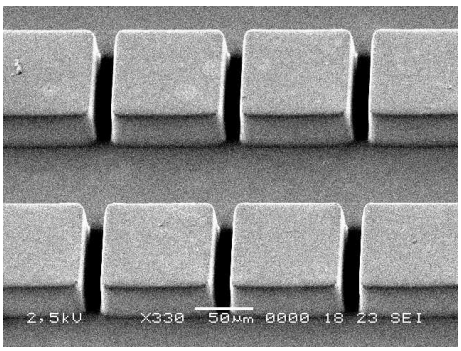
Figure 5.3: Micropatterning of PDMS via embossing.



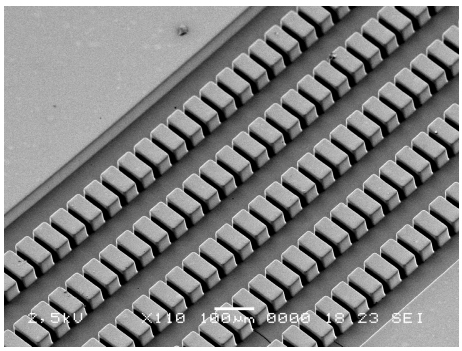
(a) Sylgard 184: 90 µm wide, 60 µm spacing.



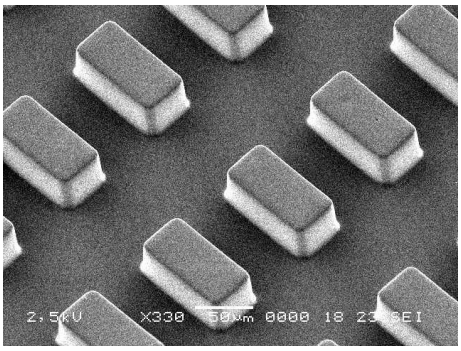
(b) Sylgard 184: 90 µm wide, 60 µm spacing.



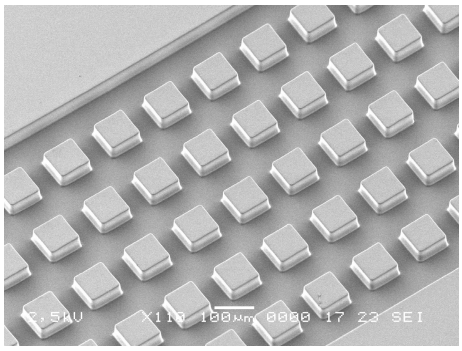
(c) Sylgard 184: 90 µm wide, 20 µm spacing.



(d) Sylgard 184: 40 µm wide, 20 µm spacing.

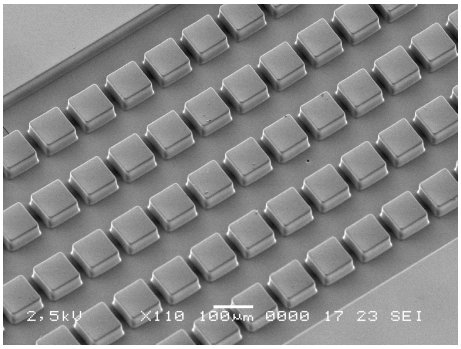


(e) Sylgard 184: 40 µm wide, 60 µm spacing.

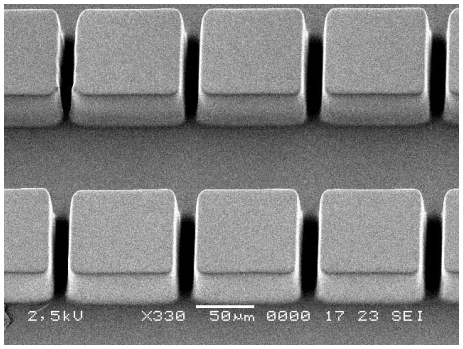


(f) Silastic MDX4-4210: 90 µm wide, 60 µm spacing.

Figure 5.4: Micropatterned surfaces (50 µm thick features) of Sylgard® 184 and Silastic® MDX4-4210.



(g) Silastic MDX4-4210: 90 µm wide, 20 µm spacing.



(h) Silastic MDX4-4210: 90 µm wide, 20 µm spacing.

Figure 5.4: Micropatterned surfaces (50 µm thick features) of Sylgard® 184 and Silastic® MDX4-4210.

face containing similar groups, e.g. activated PDMS, silicon or glass. It is hypothesized that a condensation reaction occurs, yielding covalent -O-Si-O- linkages between the two surfaces and resulting in irreversible sealing [6, 11].

In this dissertation, PDMS surfaces were activated by exposing them to air or oxygen plasmas using a Diener PICO plasma system (40 kHz generator). The power, chamber pressure and treatment time were fixed at 190 W, 0.8 mbar and 24 s, respectively. These parameters were not optimized, though they were found effective. Prolonged treatments were avoided as it has been reported that these result in the formation of an extremely brittle SiO_x layer, which cracks spontaneously or after mechanical deformation, possibly hampering successful bonding [7, 8, 12]. Another important finding which has been reported extensively is the recovery of the hydrophobic nature of the PDMS surface when the source of activation is removed. Several mechanisms have been suggested to explain this behavior, though it generally believed that the migration of low molar mass species or oligomers from the bulk to the surface is the dominant mechanism for the hydrophobic recovery [8]. Therefore, the time that elapses between the surface activation and conformal contact is minimized in order to achieve successful bonding.

In Figure 5.6, a cross section is shown of square microfluidic channels with side lengths of 100 µm, realized by bonding a micropatterned PDMS layer onto a smooth PDMS layer. The bond interface between both PDMS surfaces is indicated in Figure 5.6(b).

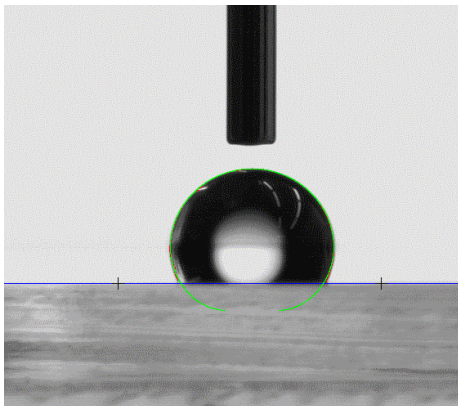
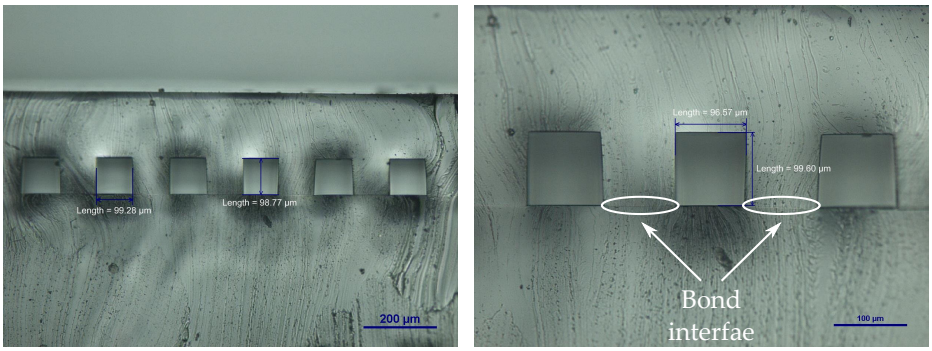


Figure 5.5: Contact angle measurement performed on Sylgard® 184.



(a) (b)

Figure 5.6: Cross section of square microfluidic channels with side lengths of 100 µm.

Type	Inner diameter [mm]	Wall dimensions [mm]
FEP, extruded (Zeus)	0.30	0.15
Silastic® Rx-80 (Dow Corning)	0.30	0.17

Table 5.4: Selected tubing; stated values are typical values [14, 15].

5.2.5 Macro-to-micro interface

At this point, enclosed microfluidic channels have been obtained. A final problem which needs to be tackled is the macro-to-micro interface, i.e. the interface between the macro-environment of the world and the microfluidic environment. Several solutions to this problem have appeared in literature; Fredrickson et al. provided a nice review on this subject [13]. Solutions range from introducing wells or reservoirs at the ends of the channels to integrated interconnects or modular interfaces. Wells or reservoirs are easily introduced, though no pressure can be applied. Integrated interconnects and modular interfaces, on the other hand, both can be used to apply pressure and allow linkage of multiple devices. Modular interfaces offer the additional advantage that they are reusable. However, these are usually device specific: either the modular interface is customized for a specific device or the other way around. Considering the pros and cons, an integrated interconnect is pursued which is leak free, allows the application of pressure and is easily assembled.

Generally, it is hard to reliably use adhesives with PDMS, either because of the low surface energy of PDMS or the possibility to clog the microfluidic channels in case of liquid adhesives. Therefore, an alternative approach is suggested which makes use of the elasticity of PDMS to mechanically clamp the tubing. To this end, coring tools are used to provide holes through a thick (> 5 mm) PDMS membrane, tubing with a matched diameter is inserted through the coring tool and the coring tool is carefully removed. For the two types of tubing mentioned in Table 5.4, a Harris Uni-core tool with an inner diameter of 0.75 mm was used. To ensure that the holes are punched at the correct positions, aligning marks can be imprinted in the thick PDMS membrane (e.g. by replica molding). The thick PDMS membrane, containing the tubing, is then manually aligned to the fluidic patterns and bonded after activating both surfaces. An example of a microfluidic device and its macro-to-micro interface, consisting of a 6 mm thick PDMS membrane, is shown in Figure 5.7.

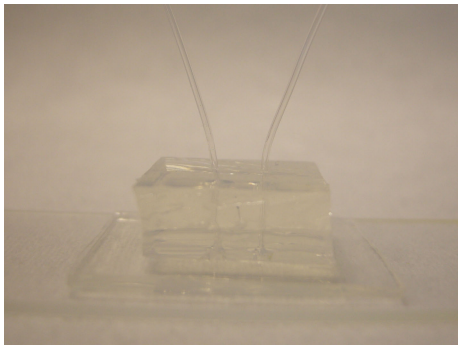


Figure 5.7: Microfluidic device and its macro-to-micro interface, consisting of a 6 mm thick PDMS membrane.

5.3 Multi-layered microfluidics

The fabrication process for multi-layered microfluidics, i.e. microfluidic devices containing two or more fluidic layers, is schematically represented in Figure 5.8. The procedure described in Section 5.2 is used to fabricate a single-layer microfluidic device (Figure 5.8(a) - Figure 5.8(c)), which is then aligned and bonded to another micropatterned PDMS membrane (Figure 5.8(d) - Figure 5.8(f)).

5.3.1 Aligning and bonding

To ease the aligning, parts A and B displayed in Figure 5.8(d) and Figure 5.8(e), respectively, are mounted in a mask aligner system (SET MG1410) using two custom-made vacuum chucks. The set-up is illustrated in Figure 5.9. One vacuum chuck is placed on the substrate table, while the other vacuum chuck is placed in the mask holder. It is ensured that both vacuum chucks are parallel to each other before mounting the samples. Next, the surfaces of part A and B are activated by exposure to an air or oxygen plasma (Figure 5.8(d) - Figure 5.8(e)), and both parts are fixated with the vacuum chucks. The positioning table and microscope of the mask aligner system are then used to align both parts before bringing them into contact and creating an irreversible bond (Figure 5.8(f)).
To achieve a successful, irreversible bond over the complete surface, it is important that both parts have a uniform thickness, and are mounted flatly on the vacuum chucks. To avoid PDMS sticking to the vacuum chucks, making flat mounting and separation after bonding difficult, a temporary carrier should be used for both parts; this is indicated in Figure 5.10. For part B, the temporary carrier should be transparent to allow alignment to the underlying features. Keeping these limitations in mind, both parts are fabricated using the embossing process

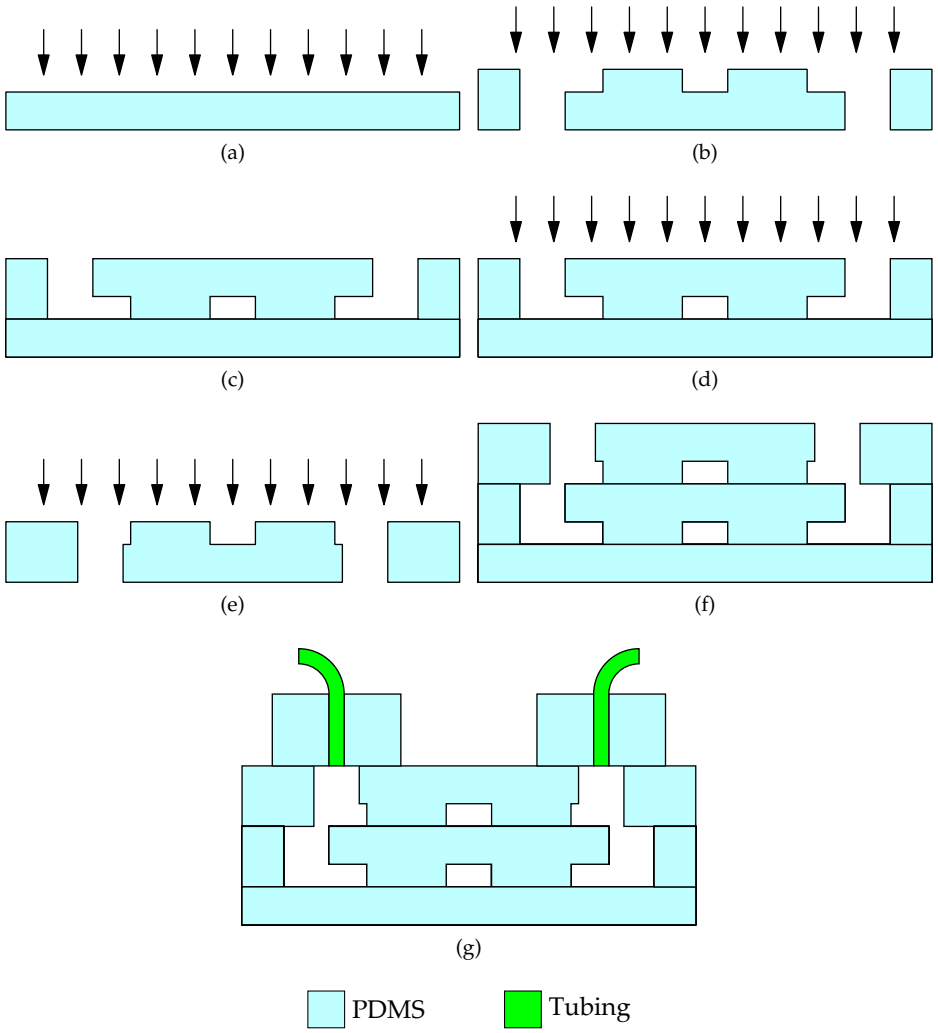


Figure 5.8: Fabrication process for multi-layered microfluidics: cross-sectional views of the fabrication steps (not drawn to scale).

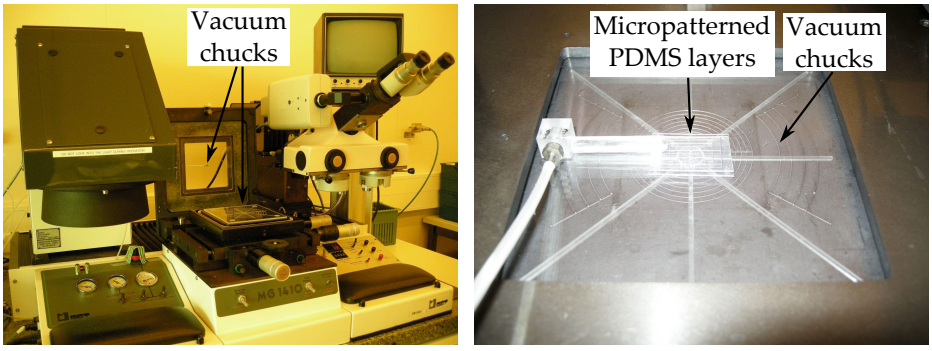


Figure 5.9: Vacuum chucks used to align two micropatterned PDMS layers, mounted on the mask aligner system (SET MG1410).

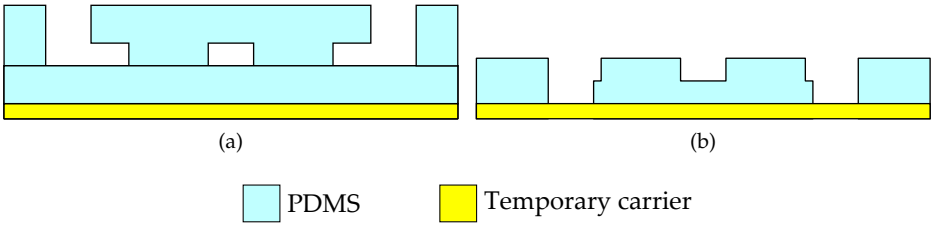


Figure 5.10: Temporary carrier for part A and B displayed in Figure 5.8(d) and Figure 5.8(e), respectively.

described in Section 5.2.3. This process ensures thickness uniformity and allows introduction of a temporary carrier.

It should also be kept in mind that PDMS has a rather high CTE ranging from 300 ppm $^{\circ}C^{-1}$ to 400 ppm $^{\circ}C^{-1}$. Curing and peeling the PDMS membrane from the master mold results in shrinkage, causing displacement of the features on the micropatterned PDMS membrane and limiting the aligning accuracy. Several measures have already been used to restrict the variations in the lateral dimensions. These include modifying the PDMS material, curing PDMS at room temperature, designing devices with large tolerances to aligning errors or accounting for the shrinkage by a design offset [16–19]. However, PDMS is not easily chemically modified, takes a few days to cure at room temperature and generally is still subject to shrinkage in spite of these measures. Designing devices with large tolerances to aligning errors may be outright undesirable, while the use of design

Cure temp [°C]	Δd_{AB} [µm]	Δd_{BC} [µm]	Δd_{CD} [µm]	Δd_{DA} [µm]	SR [%]
60	26.0 ± 1.51	28.0 ± 1.24	22.8 ± 9.16	24.7 ± 2.06	0.041
80	77.7	55.7	53.4	57.8	0.098
100	109.6	83	95.5	79.5	0.147

Table 5.5: Characterization of the shrinkage of 400 µm thick micropatterned PDMS membranes, fabricated using the embossing process and supported by a temporary carrier.

offsets is an iterative method as the degree of shrinkage depends on many factors such as cure temperature and time, membrane thickness, features, etc. Moraes et al. suggested the 'sandwich mold fabrication', i.e. the embossing process with temporary carrier as described in Section 5.2.3 [18, 20]. As the PDMS is not released from the temporary carrier, the lateral shrinkage is constrained.

To test the latter methodology, a master mold with 50 µm thick SU-8 features was fabricated, and 400 µm thick PDMS membranes (Sylgard® 184) were micropatterned using the embossing process described in Section 5.2.3. A transparent PET foil was used as temporary carrier. The PDMS was cured for 2 h at elevated temperatures of 60 °C, 80 °C and 100 °C while a pressure of approximately 100 kPa was applied on the stack. After peeling the complete stack consisting of the PDMS membrane and the temporary carrier, the features located at the corners of a 65.2 mm by 59.8 mm rectangular area on the micropatterned PDMS membrane were compared to the corresponding features on the SU-8 master mold. To this end, the distances between 'A', 'B', 'C' and 'D' (Figure 5.11) were measured both on the SU-8 master mold (e.g. $d_{AB_{SU-8}}$) and the micropatterned PDMS membrane (e.g. $d_{AB_{PDMS}}$), and subtracted from each other (e.g. $\Delta d_{AB} = d_{AB_{SU-8}} - d_{AB_{PDMS}}$). The results are summarized in Table 5.5. It is noticed that the PDMS shrinkage still depends on the cure temperature; it is quantified by the shrinking ratio SR, defined as [19]:

$$\text{SR [\%]} = \frac{1}{4} \times \left(\frac{\Delta d_{AB}}{d_{AB_{SU-8}}} + \frac{\Delta d_{BC}}{d_{BC_{SU-8}}} + \frac{\Delta d_{CD}}{d_{CD_{SU-8}}} + \frac{\Delta d_{DA}}{d_{DA_{SU-8}}} \right) \times 100 \qquad (5.1)$$

The shrinking ratio for the different cure temperatures is mentioned in Table 5.5. Shrinking ratios reported in literature for micropatterned PDMS membranes prepared simply by the cast, cure and peel process range from 0.7 % to 2.5 %, depending on the exact processing conditions [18, 19]. It is thus concluded that the proposed method effectively restrains the shrinkage of micropatterned PDMS membranes.

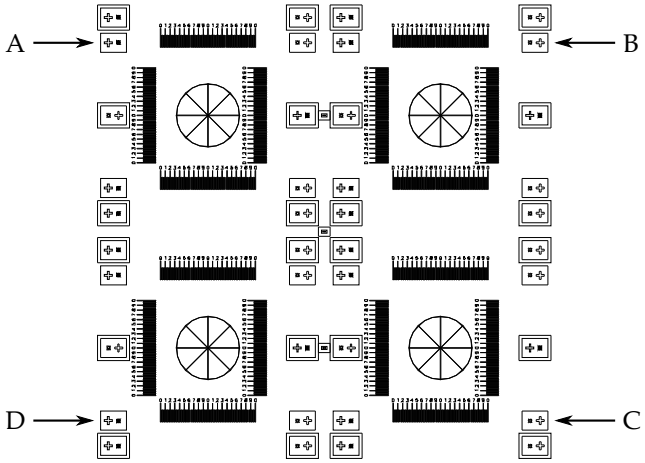


Figure 5.11: Mask design used to characterize the shrinkage of micropatterned PDMS membranes, fabricated using the embossing process and supported by a temporary carrier.

5.3.2 Integration of membranes

Since its first appearance, microfluidics rapidly developed into a versatile technology. Nowadays, microfluidic chips are used in various areas of application and incorporate different operations. Applications in the field of analytical chemistry, for example, often require sample pretreatments such as the selective removal of components (e.g. fragments with a certain size, impurities or proteins), increase of sample concentration, etc. Membranes, in this dissertation ambiguously defined as semi-permeable barriers, are highly desirable for these operations [21]. Furthermore, membranes are also of interest in fields such as gas sensors, cell culturing and fuel cells.

Depending on the transport mechanism, dense and porous membranes can be distinguished. For dense membranes, the transport occurs through the material itself, while for porous membranes, the transport occurs through empty spaces in the membrane or the pores. A typical example of the former are PDMS membranes, as PDMS is highly permeable to different gases such as nitrogen, oxygen or carbon dioxide [21–23]. Several papers also report on the in-house fabrication of porous PDMS which allows for easy integration into microfluidic devices e.g. by plasma bonding [24–27]. However, in this dissertation, focus will be put on commercially available porous membranes because of their wide variety, but also for reasons which will become clear in Section 6.3.1.

Many different approaches have been reported to integrate membranes into microfluidic environments; these were reviewed by de Jong et al. [21]. The most

straightforward approach, also pursued in this dissertation, consists in clamping or gluing the membrane between different layers with microfluidic layouts. This approach is of interest as it requires no know-how on the membrane fabrication, but also because of its polyvalence. Depending on the specific needs of the target application, the most suitable membrane can be selected, either commercially available or fabricated in-house.
Direct incorporation of membranes with PDMS-based microfluidics have already been achieved in several ways. One method involves the use of thin adhesive layers which act as an intermediate gluing layer to bond the two micropatterned PDMS layers and the membrane. Often, liquid PDMS prepolymer is used as the adhesive by transferring thin layers to the micropatterned PDMS layers as well as to the edges of the membrane by stamping [28–31]. However, this method is greatly dependent on the skills of the operator, and can easily result in the partial clogging of membrane pores or channel features. An alternative method is based on the chemical surface modification of the membrane by coating it with organo-functional silanes such as 3-aminopropyltriethoxysilane (APTES) or 3-aminopropyltrimethoxysilane (APTMS). By subsequently exposing the modified membrane surface to an oxygen plasma and conformally contacting with activated PDMS surfaces, an irreversible bond is obtained [32–35]. Although this route facilitates the integration of membranes, it has been reported that the bond strength degrades over time in aqueous environments, eventually resulting in bond failure [36]. Other methods include the encapsulation of membranes in between two micropatterned PDMS membranes, or the bonding after surface activation by exposure to oxygen plasma [25, 31, 37]. However, the former often suffers from leakage along the edge of the membrane since the membrane is not bonded but constrained at the edges by the PDMS bond, while the latter only results in a strong bond with certain membranes.
In what follows, yet another methodology is used in which thin films of SiO_2 are deposited on the membrane, allowing for direct plasma bonding [38, 39]. This dry bonding methodology can be applied to diverse materials provided that thin films of SiO_2 can be deposited on and adhere well to the material. It avoids the use of liquid adhesives, thereby also avoiding the risk of partially clogging the membrane pores or channel features. Furthermore, it facilitates the integration of membranes, while the bond strength does not degrade over time.

Fabrication process

The fabrication process for the integration of membranes using SiO_2 coatings is displayed in Figure 5.12. In theory, this process is applicable to any type of membrane, while maintaining its porosity. In this dissertation, it is applied to track-etched polycarbonate membranes purchased from it4ip; this choice will be elucidated in Section 6.3.1. It has to be noted that these porous membranes are typically very thin, with thicknesses ranging from a couple of micrometers to several

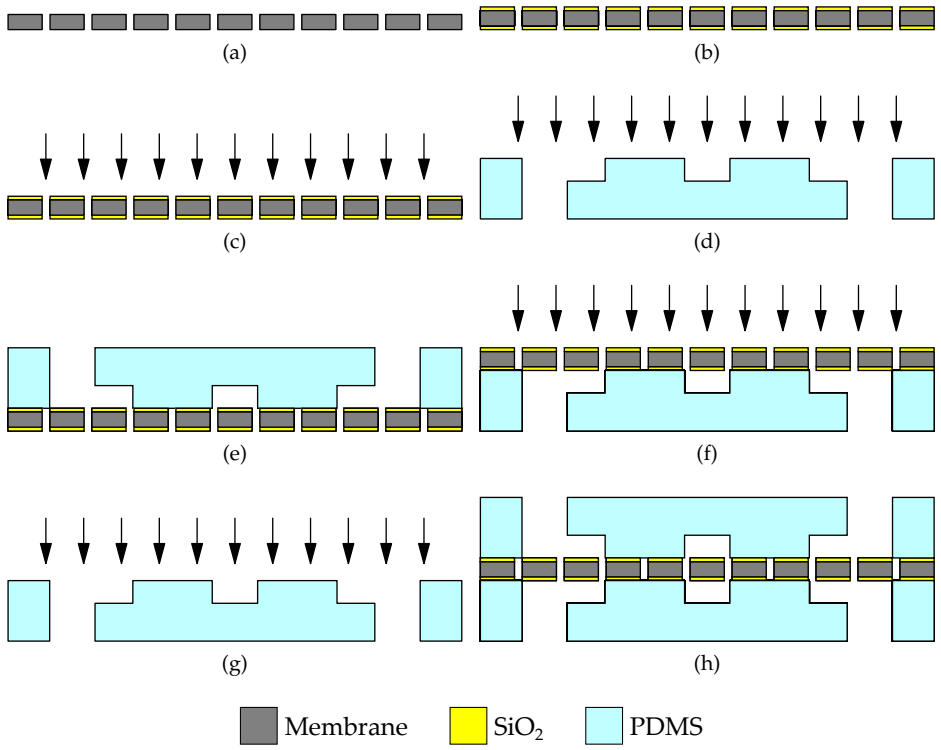


Figure 5.12: Fabrication process for the integration of membranes into PDMS-based microfluidics using SiO_2 coatings.

tens of micrometers. They are thus handled with great care during processing.

The process is started by cleaning the polycarbonate membranes using an isopropyl alcohol and deionized water soak sequence. This cleaning procedure was found inevitable to achieve a good adhesion between the SiO_2 coating and the membrane. A 50 nm thick film of SiO_2 is deposited via e-gun evaporation on both sides of the membrane (Figure 5.12(b)); the parameters are summarized in Table 5.6. The membrane is then bonded to the first micropatterned PDMS layer by exposing the corresponding surfaces to an oxygen plasma and applying the procedure described in Section 5.2.4 (Figure 5.12(c) - Figure 5.12(e)). Next, the other side of the membrane and the second micropatterned PDMS layer both are exposed to an oxygen plasma, and the microfluidic features are aligned and bonded using the procedure described in Section 5.3.1 (Figure 5.12(f) - Figure 5.12(h)). Results achieved using this procedure are shown in Section 6.3.1.

Step #	Description	Parameters
(a)	USA in a beaker with IPA	5 min
	USA in a beaker with DI	5 min
	Dry with nitrogen flush	
(b)	Evaporate SiO_2	Thickness: 50 nm,
	(both membrane sides)	Chamber pressure: 2.5×10^{-6} mbar,
		Deposition rate: 1 Å s^{-1}

Table 5.6: Process parameters to deposit SiO_2 on the polycarbonate membranes.

5.4 Integration of electronics

For some applications, it is interesting to add electronics (e.g. sensors) to the microfluidic devices. In this dissertation, the combination of PDMS-based microfluidics with the technology presented in Chapter 4 was illustrated. Therefore, as a proof of concept, a first technology demonstrator was fabricated comprising a light source and detector integrated on both sides of a microfluidic channel. A 1x4 multimode vertical-cavity surface-emitting laserdiode (VCSEL) array chip (U-L-M Photonics) was used as light source and a 1x4 photodiode (PD) array chip (Albis Optoelectronics AG) as detector [40, 41].

5.4.1 Fabrication process

The fabrication process for the integration of electronics is displayed in Figure 5.13. First, both the VCSEL and the PD array chips were thinned to 20 µm thickness and packaged using a procedure similar to the one described in Chapter 4 (Figure 5.13(a)). However, the exact fabrication process differed somewhat: the thin dies were placed in a polyimide cavity, copper metallization was used instead of gold metallization and the polyimide films were not structured to introduce stretchability; the exact fabrication process is described in detail by Missinne et al. [42]. PDMS (Sylgard® 184) was then spin coated at 700 rpm for 60 s on the top polyimide film of both the VCSEL and PD array chips packages, resulting in a layer of approximately 70 µm thickness (Figure 5.13(b)). Prior to application of the PDMS, 1200 OS Primer was applied according to the procedure described in Section 3.2.8, to promote the adhesion between PDMS and polyimide. The PDMS was kept at room temperature on a leveled platform for 24 h, allowing for maximum planarization, and subsequently thermally cured on a hotplate for 60 min at 60 °C.
The micropatterned PDMS layer was prepared using the procedure described in Section 5.2.3. The corresponding surfaces on both the micropatterned PDMS layer and the packaged VCSEL array chip are then exposed to an oxygen plasma,

and aligned and bonded using the procedure described in Section 5.3.1 (Figure 5.13(c) - Figure 5.13(e)). Next, the same is repeated for the other side of the micropatterned PDMS layer and the packaged PD array chip, and the latter is aligned to the VCSEL array chip and the microfluidic channel (Figure 5.13(f) - Figure 5.13(h)).

5.4.2 Technology demonstrator

In Figure 5.14, some pictures of the realized technology demonstrator are shown. It is clearly illustrated that the circular active areas of the four VCSELs are centered beneath the microfluidic channel (Figure 5.14(b)). Figure 5.14(c) illustrates the finished technology demonstrator; the VCSEL and PD array chips are aligned to the microfluidic channel and each other.
Measurements illustrate the optical coupling between the VCSELs and the opposing PDs. The VCSELs emit light by sourcing current (step size: 0.1 mA), while the light is detected by the respective facing PDs. The measurements were performed with a microfluidic channel which was filled both with deionized water and a solution containing microspheres of 1 µm (Polybead® Dyed Microspheres, Polysciences). The optical coupling is graphically represented in Figure 5.15 for two pairs of VCSELs and PDs. In case the solution containing microspheres is flushed through the microfluidic channels, a small ripple on the optical coupling is noticed, indicating scattering of the emitted light beam caused by the microspheres. A VCSEL and PD, combined in such an arrangement, could actually be used to detect the movement of particles. However, this was not further investigated within the frame of this PhD research.

5.5 Conclusions

Two basic techniques have been described which enable the fabrication of single-layer PDMS-based microfluidics: one technique for the micropatterning, and a second technique for the bonding of PDMS layers. For the micropatterning of PDMS, soft-lithographic techniques were used to replicate the relief structures present on the surface of well-defined master molds. These master molds were fabricated via SU-8 photolithography, allowing for thick, high-aspect ratio polymer features. The second technique, the bonding of micropatterned PDMS layers, is based on surface modification using plasma treatments, and result in irreversible bonds. Communication with the macro-environment is enabled via a customized, reliable macro-to-micro interface.
The fabrication process was extended to multi-layer microfluidic devices by introducing an aligning technique for multiple micropatterned PDMS layers. A temporary carrier was introduced to support the micropatterned PDMS layers, thereby minimizing the aligning error caused by shrinkage of PDMS during curing. Using this temporary carrier, shrinking ratios as low as 0.041 % have been

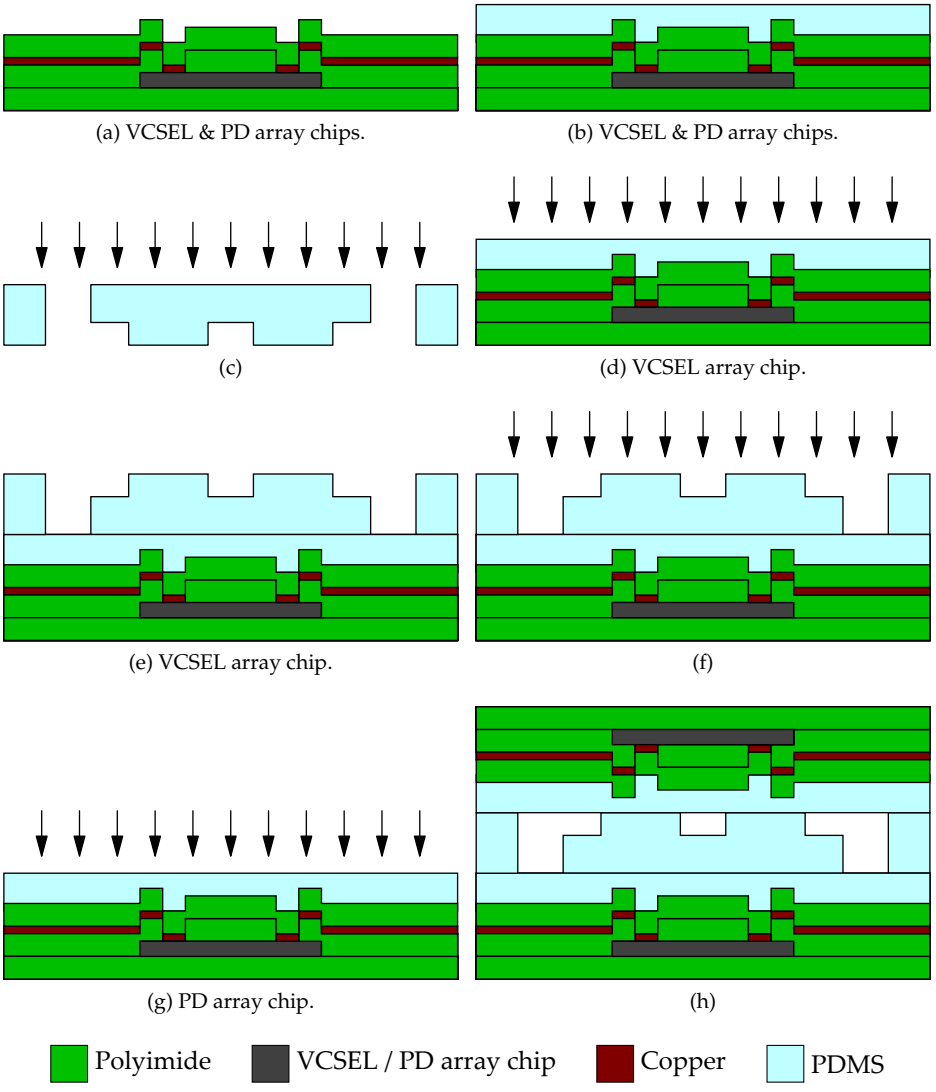
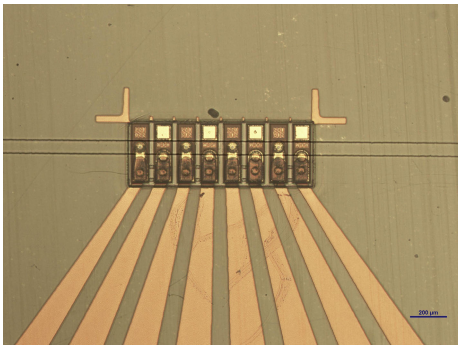
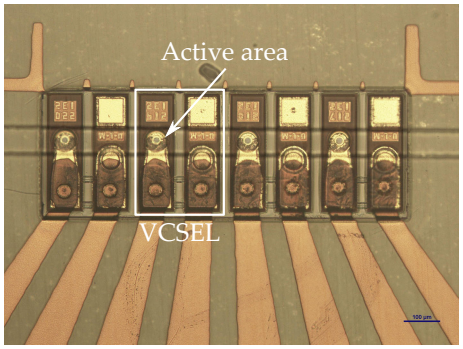


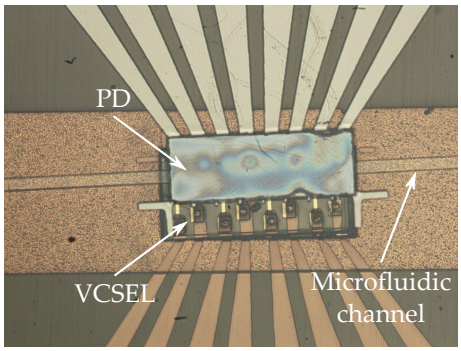
Figure 5.13: Fabrication process for the integration of electronics with PDMS-based microfluidics.



(a) Microfluidic channel aligned and bonded to the packaged VCSEL array chip.

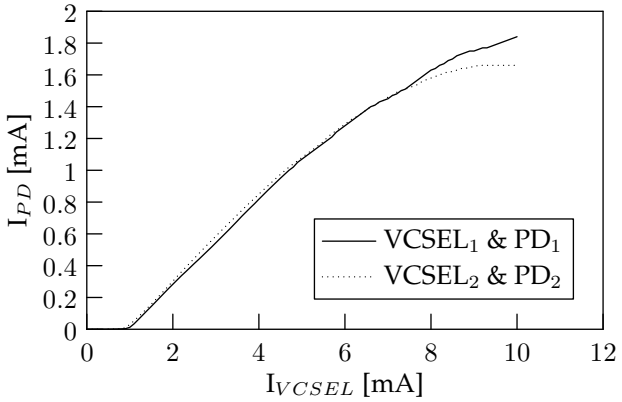


(b) Microfluidic channel aligned and bonded to the packaged VCSEL array chip.

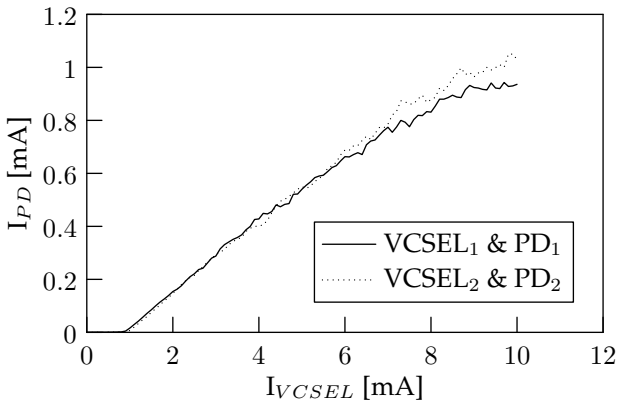


(c) VCSEL and PD array chips aligned to the microfluidic channel.

Figure 5.14: Technology demonstrator illustrating the integration of electronics with PDMS-based microfluidics.



(a) Microfluidic channel filled with deionized water.



(b) Microfluidic channel filled with a solution containing microspheres of 1 µm.

Figure 5.15: Optical coupling between VCSEL and PD, located at both sides of a microfluidic channel.

illustrated. In addition, this technique was used to allow the integration of membranes in between multiple fluidic layers. These are integrated using thin films of SiO_2, deposited on the membrane and allowing for direct plasma bonding.
Lastly, a methodology has been described to add electronics to PDMS-based microfluidic devices. Particular attention has been spent to combine the PDMS-based microfluidics with the technology presented in Chapter 4. As a proof of concept, a technology demonstrator was fabricated comprising a light source and detector integrated on both sides of a microfluidic channel.

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6
Enabling applications

6.1 Introduction

Whereas in previous chapters, technologies for the realization of stretchable electronics and PDMS-based microfluidics were presented, in this chapter applications are highlighted which benefit greatly from these technologies. In the first section of this chapter, elastic microsystems with modular functionalities are discussed. Focus is put on the developments and preliminary results which were achieved within the frame of the IWT-SBO funded project BrainSTAR, which aims to develop wireless microsystems for **brain st**imulation **a**nd **r**ecording in small animal models. The next section focuses on the use of PDMS-based microfluidics for cell culturing. Focus is put on the developments and preliminary results achieved within the frame of the IWT-SBO funded project HEPSTEM, which aims to develop functional human **hep**atocytes, stellate cells and sinusoidal endothelial cells from **stem** cells.

6.2 Elastic microsystems with modular functionalities

In Chapter 1, diverse applications benefiting from stretchable electronics have been introduced. In this dissertation, an architecture of functional modular islands interconnected by stretchable electrical wiring is pursued. This strategy is employed to develop the system envisioned within the frame of the IWT-SBO funded project BrainSTAR, which is an acronym for "wireless microsystem for

brain stimulation **a**nd **r**ecording in small animal models".

6.2.1 BrainSTAR

Implantable neural microsystems provide an interface to the nervous system, giving cellular resolution to physiological processes unattainable today with non-invasive methods. They can be used in neuroscience to understand physiological processes or in neural prosthetics to help restore and / or support neuromuscular and neurosensory systems. Cardiac pacemakers and cochlear implants are the perfect example of already commercially available prosthetics in neuromuscular and neurosensory support, respectively. Furthermore, chronic deep brain stimulation (DBS) proved to be extremely effective for the treatment of many disorders, such as Parkinson's disease, dystonia, epilepsy, depression and obsessive-compulsive disorder. The importance of brain-lesion cavities in humans cannot be overestimated. It suffices to say that lesion cavities in the brain are seen in many neurological and neurosurgical disorders. Some examples are stroke, brain trauma, congenital brain disorders and final results after successful treatment of brain tumors or abscesses. DBS techniques may also have a significant impact in the treatment of such lesions.
For the development and testing of new medical, neurosurgical and pharmacological treatments, research cannot begin with human subjects. Strong similarities are however seen between certain animal species and the human with respect to brain function. Therefore, at the early stages, typically small animals are used: rat or transgenic mice. The small animal case mainly differs from the human case with respect to the animal and relative brain size. Small animals will thus impose harder miniaturization constraints for the overall system but not for the neural probe itself (local brain structures are similar). Restrictions are imposed regarding volume, dimensions and weight. Rats and mice easily differ by a factor of 10 in weight, imposing even larger constraints on the mice implant.
The ideal implant should not restrict the animal physically since this may introduce different behavior or even stress which would be detrimental regarding the investigation of psychiatric diseases or learning / memory effects. Still, most animal experiments are carried out using large mechanical swivel constructions, bulky connectors and cables, and heavy backpack, collar, or saddlebag solutions (Figure 6.1). Implantable solutions with the same functionality as the wired devices are not available yet but are thus highly advantageous.
The overarching goal of BrainSTAR is to develop a novel wireless microsystem supporting multi-channel artifact-free brain stimulation and recording in small animals. Important aspects for the application in small rodents are:

- the miniaturization of the recording / stimulation probe array to an implantable size;
- the replacement of any cables by wireless connection to allow animals to

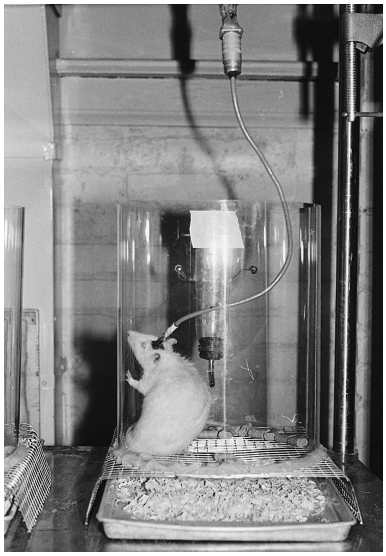


Figure 6.1: Swivel-based cage solution [1].

move and behave freely without being significantly affected by the experimental setup;

- overall miniaturization to allow for compactness and lightweight;
- suitable placement, packaging and interconnect of all system components without inducing stress on the animal.

The generic technology presented in Chapter 3 and Chapter 4 is taken up to enable a system for the specific context of neural interfaces. The envisioned system is schematically represented in Figure 6.2; the position of each system part relative to the animal's body is indicated. The silicon neuroprobe is electrically connected to an ASIC which is embedded as thin die in polyimide to limit the weight and volume, but also to improve flexibility near the head. The ASIC is designed to address the signal handling, including both analog and digital signal pre- and post-processing for the neuronal stimulation and the recorded neural signals. At the back of the system, another flexible island contains a power supply (e.g. battery), wireless module, signal conditioning, etc. These modules are assembled using conventional techniques. Meandering metallic conductors connect both flexible islands, and allow for stretchability and thus increased comfortability. As indicated in Figure 6.2, the system is partially encapsulated in a silicone elastomer. A biomedical grade PDMS is considered for this purpose to retain the possibility to subcutaneously implant the entire or part of the system.

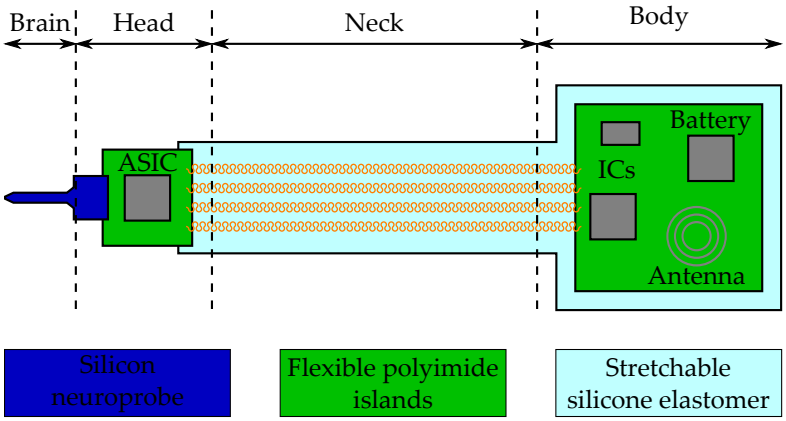


Figure 6.2: Schematic representation of the envisioned system within BrainSTAR.

6.2.2 Technology demonstrator

To illustrate the applicability of the technologies presented in Chapter 3 and Chapter 4 for the envisioned system in BrainSTAR, a first technology demonstrator was designed and fabricated using the MSP430F1611 microcontroller chips from Texas Instruments. It is designed to illustrate the full functionality of an electronic circuit which is built around a thinned and embedded commercially available chip, configured in a layout similar to that of the system depicted in Figure 6.2: polyimide islands hosting electronic components, either thinned and embedded, or assembled in conventional ways using conductive adhesives, are connected by stretchable wiring.

Microcontroller MSP430F1611

MSP430 16-bit mixed-signal microcontrollers from Texas Instruments are ideally suited for a wide range of low power and portable applications due to its low power consumption. This microcontroller family incorporates a 16-bit RISC central processing unit (CPU), peripherals and a flexible clock system in a Von Neumann architecture. The microcontrollers come in a variety of configurations and can feature several peripherals such as communication interfaces (I^2C, UART, SPI, etc.), timers, analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). Ultra low power functionality is obtained through the availability of several low power modes, allowing parts of the system to be temporarily disabled.
The MSP430F1611 microcontroller was chosen because of its availability as un-

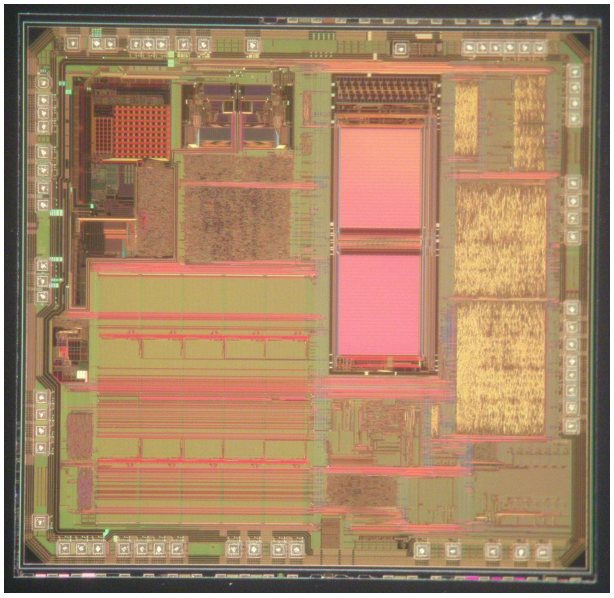


Figure 6.3: Microscope picture of a 35 µm thick MSP430F1611 microcontroller.

packaged dies at CMST. The microcontrollers were thinned down on wafer scale at DISCO HI-TEC EUROPE GmbH from an initial thickness of 725 µm, which is the standard thickness of an 8 inch silicon wafer, to a target thickness of 30 µm. To this end, a dicing before grinding (DBG) methodology (Section 2.2.3) was used. Although the target thickness was 30 µm, the microcontrollers had thicknesses ranging from 35 µm to 40 µm. A microscope picture of a 35 µm thick microcontroller is shown in Figure 6.3 and illustrates the layout. The die measures approximately 4.6 mm by 4.4 mm. The bond pads (75 µm by 75 µm) are distributed over the periphery and are ENIG surface finished by the supplier.

Design and fabrication

Two versions 'A' and 'B' of the technology demonstrator were fabricated; the electronic schematics and the mask designs are shown in Figure 6.4 and Figure 6.5, respectively. Figure 6.4(b) and Figure 6.5(b) display the design of the metallization for version A and B, respectively, clearly indicating the stretchable interconnections and footprints for the SMD components. Figure 6.4(c) and Figure 6.5(c) display the polyimide design for version A and B, respectively, clearly indicating the polyimide support for the stretchable interconnections, the rectangular openings for the footprints and the circular openings for the programming pads. Both versions contain two LEDs (SML-311UT, ROHM) and a 2-pin connector (FTR-102-

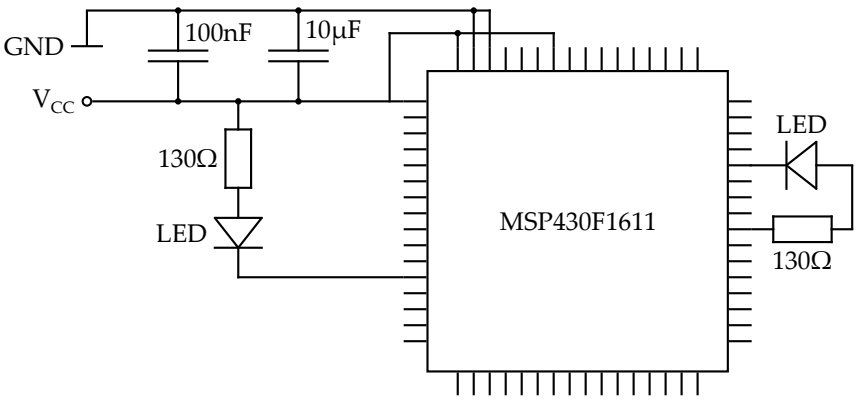
01-L-S, Samtec) which is used to connect a power supply or battery. Although the footprint for a temperature sensor (LM92CIM, National Semiconductor) is foreseen, the sensor was not assembled. For design A, digital I/O and timers are used to blink the LED on the left, while the on-chip integrated temperature sensor is used to light the LED on the right. For design B, digital I/O and timers are used to blink the LED on the left, while a capacitive touch sensor and the capacitive touch sense library are used to light the LED on the right.

A slightly altered fabrication process compared to the one described in Chapter 4 is used for the technology demonstrator; it is displayed in Figure 6.6. The customized release layer stack, described in Section 4.2.3, was omitted. This was feasible considering the small overall size of the circuit, and because the entire circuit is linked to a central flexible island, maintaining the relative position of each element of the circuit. To allow release of the circuit in a final stage of the fabrication process, the bad adhesion of polyimide PI-2611 to the glass substrates has been exploited. Selective application of adhesion promoter VM-652 (HD Microsystems^{TM}) at the perimeter of the glass substrates results in PI-2611 films which are nicely adhered at the edges, while marginal adhesion elsewhere is obtained [2]. This way, sufficient adhesion of the subsequent PI-2611 film is ensured throughout the fabrication process.

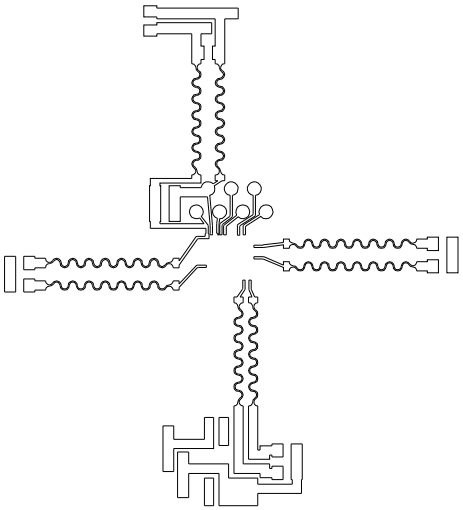
The thinned dies were placed using the procedure described in Section 4.2.5 (Figure 6.6(a)). A surface scan of a placed die was taken with an optical profiler WYKO NT3300 (Veeco), and is displayed in Figure 6.7. As noticed, the die / BCB assembly has a thickness of approximately 40 µm. In Figure 6.7(b) and Figure 6.7(c), the cross-sectional profiles of the die along its centerlines is displayed. It is observed that the die is placed quite flatly, with thickness variations of maximum 4 µm.

The die was subsequently covered by another layer of PI-2611. Although the thickness of the die slightly exceeded the 30 µm target thickness, the thickness of the covering polyimide film was retained at 5.5 µm. As indicated by the cross sections displayed in Figure 6.8, a continuous coating was obtained both at the edges of the die and around the ENIG surface finished bond pads. The polyimide film was then patterned to provide vias towards the die bond pads, using the procedure described in Section 4.2.6 (Figure 6.6(b) - Figure 6.6(c)). As the bond pads of the dies are ENIG surface finished by the provider, this step was not performed. Therefore, the next step consisted in the application of the metallization, as described in Section 4.2.8 (Figure 6.6(d)). The continuity of the metallization at the edges of the die is demonstrated in Figure 6.9. Next, another 5.5 µm thick polyimide film was spin coated and cured to cover the metallization. After patterning the polyimide, polyimide covered stretchable interconnections and polyimide islands hosting the thinned die and footprints for the SMD components ware obtained (Figure 6.6(f)).

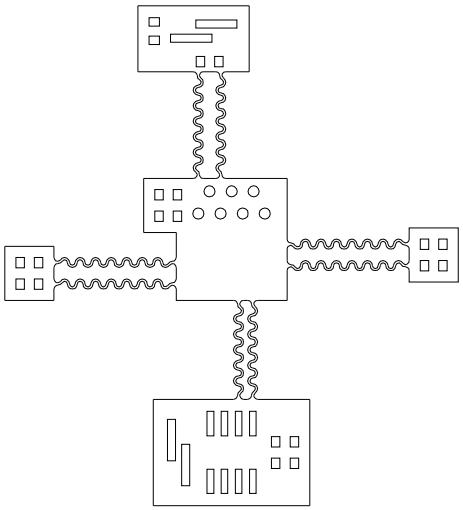
The flexible / stretchable circuit was then manually separated from the substrate (Figure 6.10(a)). This is easily done as the adhesion promoter has only been ap-



(a) Version 'A': electronic schematic.

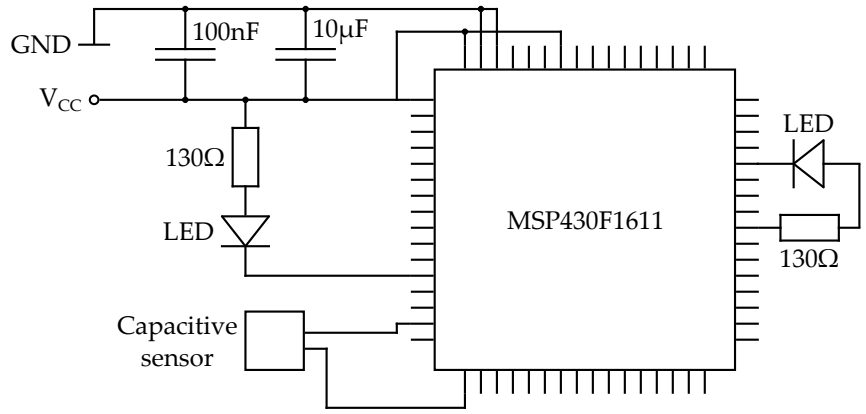


(b) Version 'A': metallization.

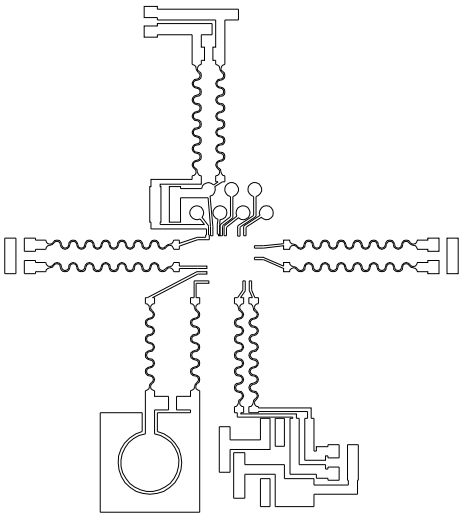


(c) Version 'A': polyimide.

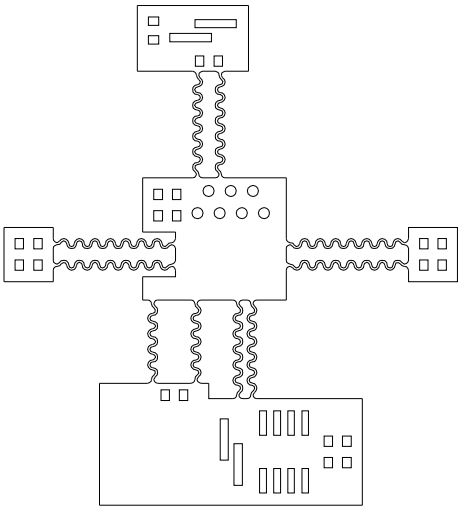
Figure 6.4: Electronic schematic and mask design of version 'A' of the technology demonstrator.



(a) Version 'B': electronic schematic.



(b) Version 'B': metallization.



(c) Version 'B': polyimide.

Figure 6.5: Electronic schematic and mask design of version 'B' of the technology demonstrator.

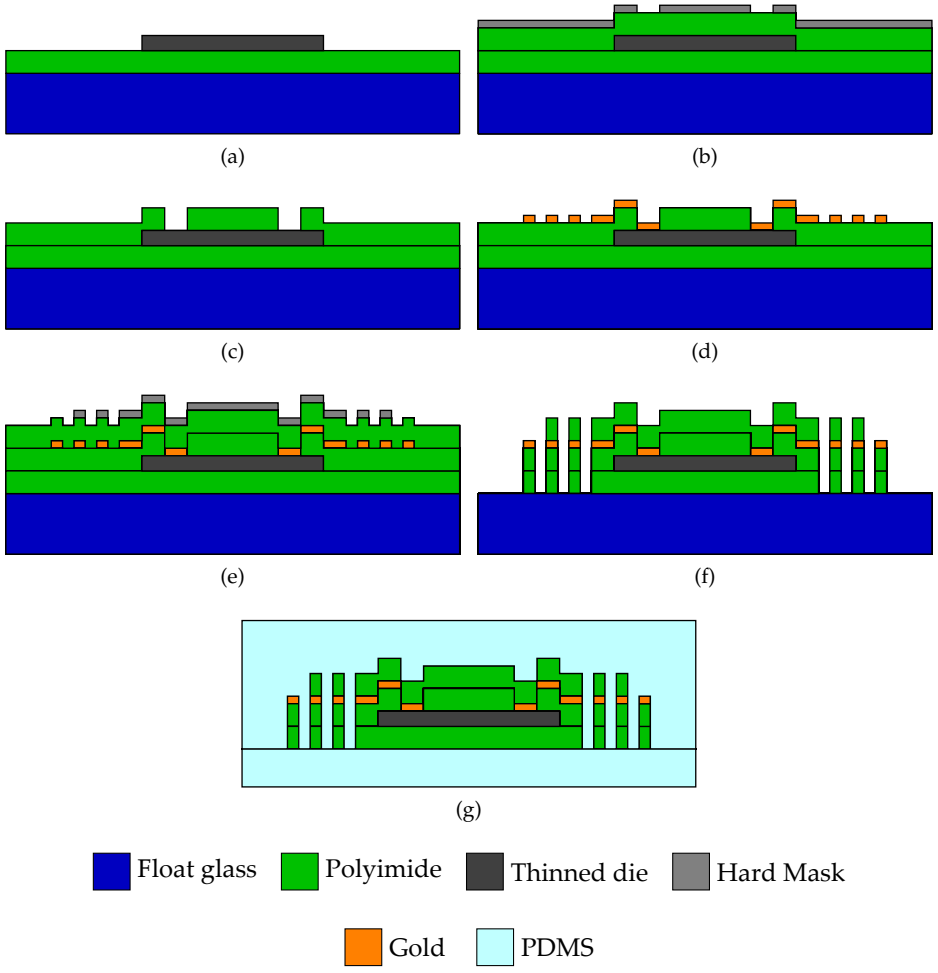
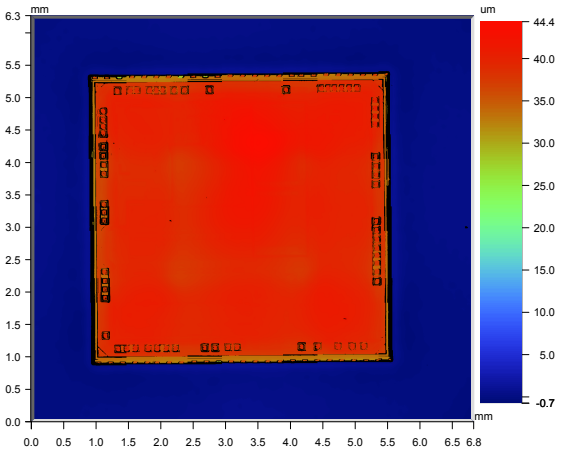
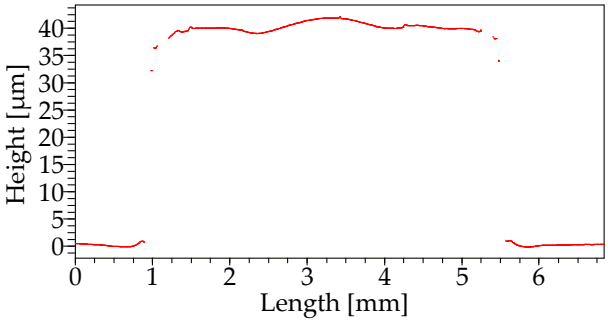


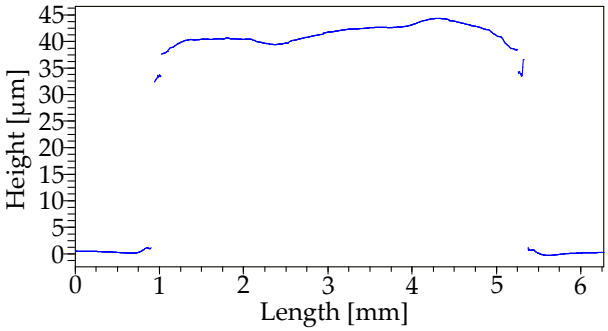
Figure 6.6: Fabrication process for the technology demonstrator containing an MSP430F1611 microcontroller: cross-sectional views of the fabrication steps (not drawn to scale).



(a) Overview.

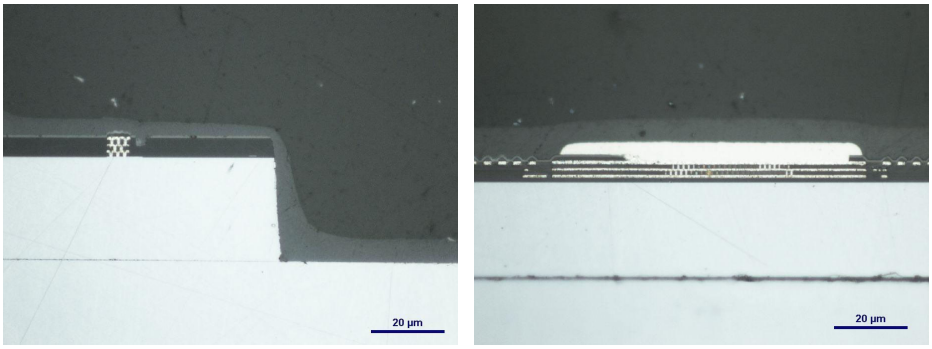


(b) Cross-sectional profile along the horizontal centerline.



(c) Cross-sectional profile along the vertical centerline.

Figure 6.7: Surface scan of flatly placed thin MSP430F1611 microcontroller dies.



(a) Edges of the die. (b) ENIG surface finished bond pad.

Figure 6.8: Cross sections of a 35 µm thick MSP430F1611 microcontroller, covered by a 5.5 µm thick PI-2611 film, and resulting in a continuous coating.

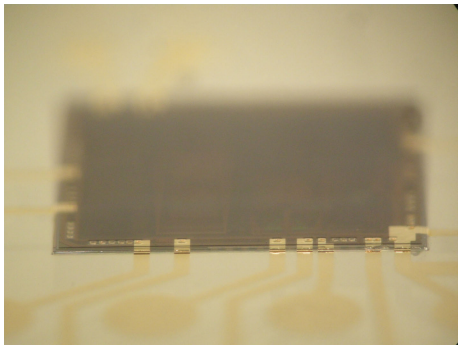
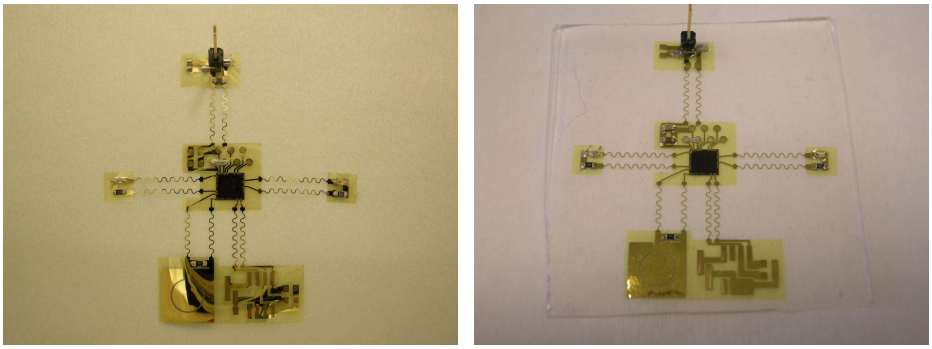


Figure 6.9: Continuity of the metallization at the edges of the die.



(a) Before encapsulation in PDMS. (b) After encapsulation in PDMS.

Figure 6.10: Released, stretchable technology demonstrator before and after encapsulation in PDMS.

plied at the edges of the substrate. The overall thickness of the circuit, including the embedded microcontroller, was as low as 50 µm. Subsequently, SMD components were assembled and the microcontroller was programmed. The SMD components were assembled by means of an isotropic conductive adhesive CE 3104 (Emerson & Cuming). This adhesive was chosen as it was found impossible to perform regular soldering without damaging the gold film because it dissolves too rapidly into the solder. The microcontroller was programmed using IAR Kickstart software [3], an OLIMEX MSP430-JTAG-TINY programmer and a homemade PCB providing a pogo pin interface towards the flexible circuit (Figure 6.11).

In the final stage of the fabrication process, the circuit was encapsulated in PDMS (Figure 6.6(g)). Silastic® MDX-4 4210 (Dow Corning) was chosen for this purpose. A 350 µm thick PDMS layer was spin coated on a glass substrate, the assembled circuit was carefully placed on top of the liquid PDMS and another 350 µm thick PDMS layer was spin coated. Although this technique was chosen because of its simplicity, it is expected that the reliability of the circuit can be increased by performing injection molding. By inserting the circuit in between dedicated molds and injecting PDMS, the PDMS thickness can be tuned near fragile regions (e.g. mounted SMD components) to limit the flexibility locally.

The embedded circuit is shown in Figure 6.10(b). In Figure 6.12, the functionality of the embedded circuit and the thinned microcontroller is illustrated. The circuit is wrapped around a cylinder with 15 mm curvature radius. As already mentioned, digital I/O and timers are used to blink the LED on the left, while the capacitive touch sensor and the capacitive touch sense library are used to light the LED on the right. In addition, the DACs, ADCs and on-chip integrated

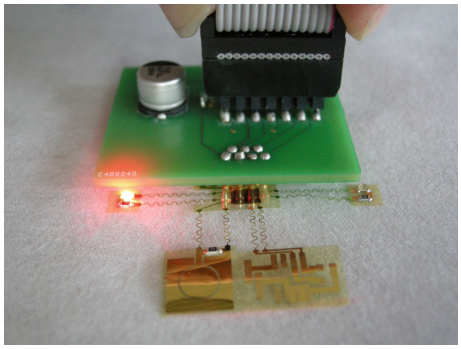


Figure 6.11: Programming of the MSP430F1611 microcontroller.

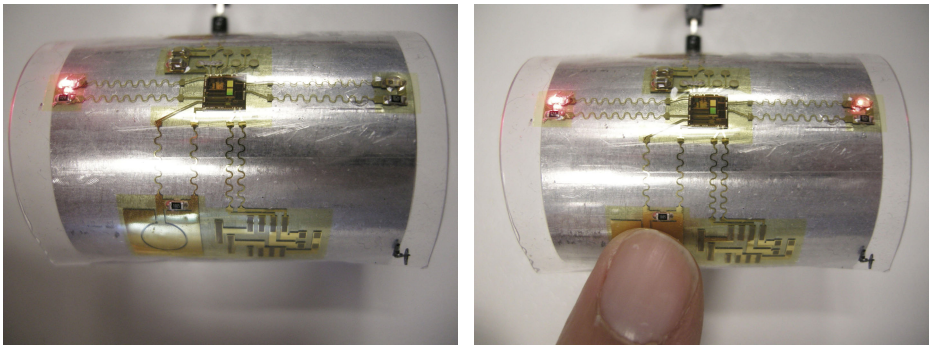
temperature sensor were verified to function well.
The embedded circuit was uniaxially stretched using the custom-built stretching setup displayed in Figure 6.13(b). As illustrated in Figure 6.13(a), the circuit still functions when stretched up to 27 % its original length. Note that the elongation of the electrical interconnections is actually larger due to the non-stretchable nature of the polyimide islands, both at the center and the edges.

6.3 Microfluidics for cell culturing

From Section 1.2, it is clear that microfluidic technologies may significantly impact research in the field of cell biology. In what follows, the relevance of microfluidics for liver-related research will be highlighted. This will be done by highlighting the research performed within the frame of the IWT-SBO funded project HEPSTEM, which is an acronym for "functional human **hep**atocytes, stellate cells and sinusoidal endothelial cells from **stem** cells".

6.3.1 HEPSTEM

The liver is the largest and main metabolic organ within the human body highly involved in the maintenance of homeostasis, i.e. keeping the body's internal environment stable. It has numerous functions, including protein synthesis, blood detoxification and production of bile. A unique feature of the healthy liver is its ability to regenerate itself when damaged, however, liver failure can occur when the normal regenerative process is compromised. End-stage liver disease is routinely treated by liver transplantation, though the shortage of donor livers remains a serious problem. Interestingly, patients with liver failure can be temporarily supported by bioartificial liver devices to bridge the period to liver transplantation, or to allow spontaneous recovering of the liver.



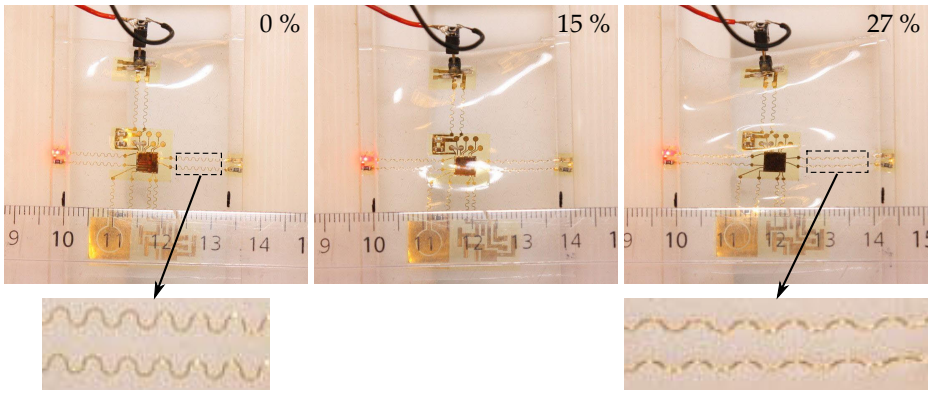
(a) (b)

Figure 6.12: Embedded circuit wrapped around a cylinder with 15 mm curvature radius.

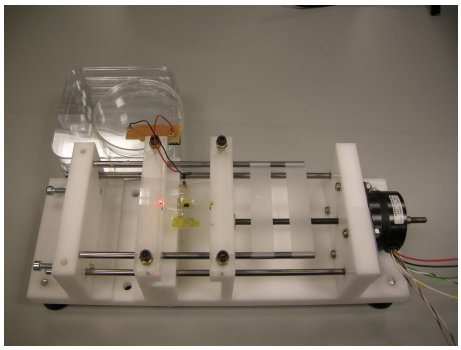
The overarching goal of HEPSTEM is to develop mature, functional hepatocytes from human pluripotent stem cells (embryonic stem cells (ESC) and induced pluripotent stem cells (iPSC)). Such cells could be used:

- by the pharmaceutical industry to evaluate drug metabolism and study mechanisms underlying hepatitis B virus and hepatitis C virus infection;
- in bioartificial liver (BAL) devices that can support detoxification functions of the liver to bridge patients with acute liver failure to liver transplantation;
- as source of cells for hepatocyte transplantation, even though this is likely the most difficult to reach.

Researchers have previously differentiated stem cells towards hepatocyte-like cells, however, not much attention was spent to the highly specialized nature of the liver architecture. The cellular architecture of the liver is displayed in Figure 6.14. Hepatocytes are arranged in cords between the capillaries (sinusoids) of the liver, and are flanked by highly specialized fenestrated hepatic sinusoidal endothelial cells (HSEC), hepatic stellate cells (HSC) and Kupffer cells, which influence the differentiation and the function of hepatocytes. It is hypothesized that the generation of fully functional hepatocytes will require a close mimicking of the highly specialized nature of the *in vivo* hepatic sinusoid. Therefore, one of the objectives within HEPSTEM is the development of a "micro-hepatic sinusoid bioreactor" wherein specific cell-cell interactions between developing hepatocytes and accessory cells can be followed at the single cell level.



(a)



(b)

Figure 6.13: Uniaxial stretching of the embedded circuit up to 27 % its original length, using a custom-built stretching setup.

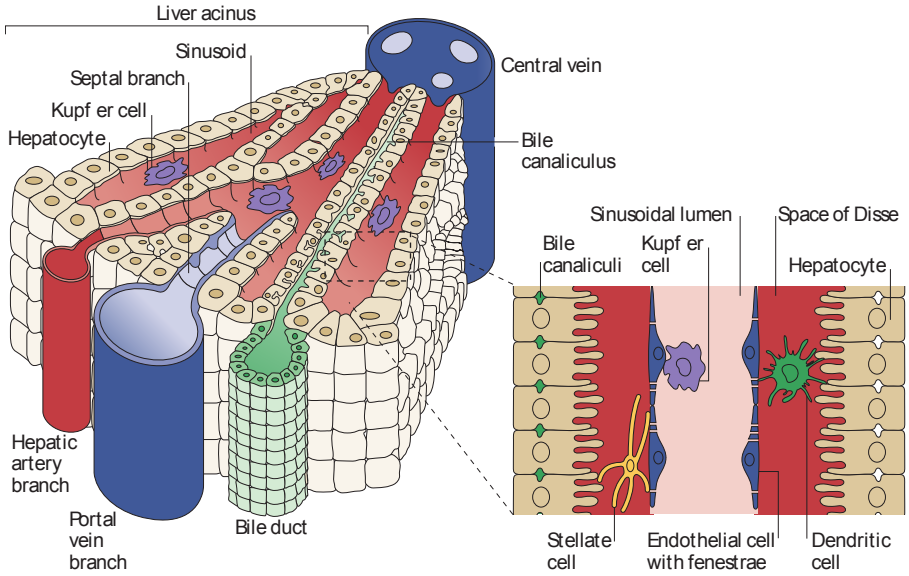


Figure 6.14: Cellular architecture of the liver [4]. Hepatocytes are arranged in cords between the capillaries (sinusoids) of the liver, and are flanked by highly specialized fenestrated hepatic sinusoidal endothelial cells, hepatic stellate cells and Kupffer cells (see inset). The hepatocytes are thus separated from blood by sinusoidal cells and are only exposed to plasma, allowing the exchange of plasma proteins, nutrients and metabolites.

6.3.2 Micro-hepatic sinusoid bioreactor

Configuration

There are three criteria governing the envisioned micro-hepatic sinusoid bioreactor. The bioreactor should (a) have an architecture closely resembling that of the liver *in vivo*, (b) confine different cell populations to individual compartments from which they cannot 'escape', while allowing 'natural' cellular (chemical and physical) communication between the different cell populations and (c) accurately provide oxygen and nutrients to the different cells. A schematic representation of the cross section of the envisioned microfluidic bioreactor is displayed in Figure 6.15. It consists of multiple PDMS microfluidic layers, separated by porous membranes, and allowing co-culture and juxtaposition of two cell types, i.e. hepatic sinusoidal endothelial cells and hepatocytes. PDMS is of particular interest because of its:

- Transparency / translucency, allowing for optical monitoring of cells in the microfluidic environment.
- Ease of processing.
- Ability to easily and reliably stack multiple PDMS microfluidic layers.
- Possibility to integrate porous membranes (Section 5.3.2).
- Possibility to integrate sensors in the microfluidic channels (Section 5.4).
- High permeability to gases such as oxygen contribute to the provision of oxygen to the different cells [5, 6].

Shear stress is known to affect cell structure, growth and function. While endothelial cells are continuously subject to laminar shear stresses *in vivo*, hepatocytes are preferably shielded from shear stress to avoid its detrimental effects on hepatocytes [7–9]. Therefore, the hepatic sinusoidal endothelial cells are seeded in the flow channels and are thus directly subject to fluidic shear stress, while nutrients diffuse through the porous membrane towards the hepatocytes which are thus shielded from shear stresses. The small dimensions of the microchannels ensure laminar fluid flow, even at very high fluid velocities. Assuming Poiseuille flow in the microchannels, the shear stress at the wall τ_w of the microchannels can be estimated by:

$$\tau_w = 6\mu \frac{Q}{h^2 w} \tag{6.1}$$

with μ the dynamic viscosity of the fluid, Q the fluid flow rate, h the height of the microchannel and w the width of the microchannel [10]. By altering the fluid flow

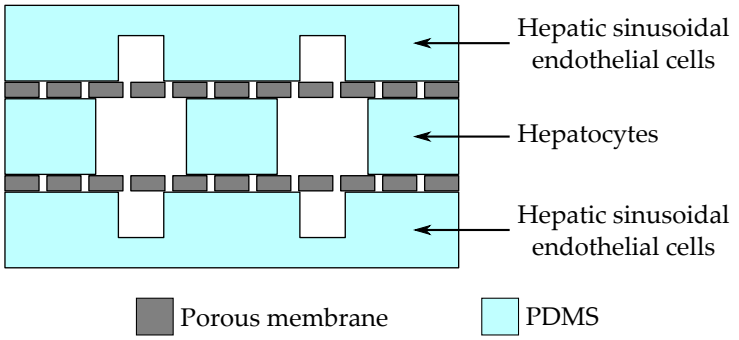


Figure 6.15: Schematic representation of the cross section of the envisioned microfluidic bioreactor. The target dimensions for the square microfluidic channels for the hepatic sinusoidal endothelial cells and hepatocytes, 20 µm and 100 µm, respectively, are in the same order of magnitude of the respective cell sizes.

rate and the geometry of the microchannels, the shear stress can thus be adjusted to match physiological values.
Considering the criteria for the bioreactor, there are different requirements for the porous membranes.

- Non-toxicity.
- Conducive to cell adhesion: proper cell adhesion is required to avoid the cells being flushed away by the fluid.
- Small membrane thickness: as small as possible, allowing juxtaposition of hepatic sinusoidal endothelial cells and hepatocytes, thus better mimicking the *in vivo* situation.
- Small pore size: taking into account a margin which covers the ability of the cells to deform, the pore diameters should not be larger than ~3 µm to prevent cell migration across the membrane and thus to confine the different cell populations their compartments.
- High pore density: not exactly specified, though it is expected that high pore density is desirable.
- Ability to monitor optically: the ability to optically monitor cell growth and morphology through the porous membrane (e.g. by optical microscopy) is advantageous. The porous membrane is thus preferably transparent or translucent.

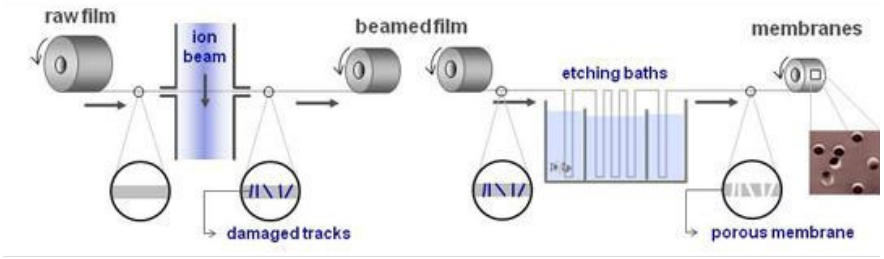
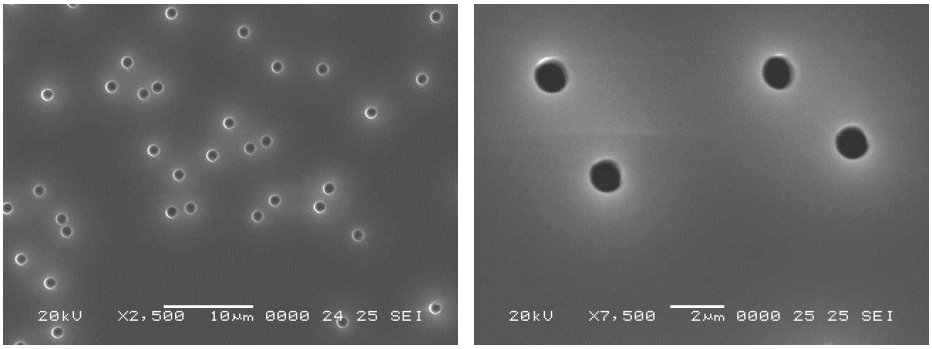


Figure 6.16: Ion track-etching technology to produce porous membranes [11].

Figure 6.17: Range of pore sizes and pore densities [11].

The latter requirement limits the choice of porous membranes greatly, though track-etched membranes are an excellent choice for this purpose. The ion track-etching technology and its different processing steps is displayed in Figure 6.16. Using this technology, micro- and nano-pores with high aspect ratio can be prepared in many polymer membranes by irradiating them with energetic heavy ions. So-called latent ion tracks are formed when ions hit and penetrate the polymer, resulting in a permanent modification of the physical and chemical properties along the linear path. The latent ion tracks are subsequently preferentially wet chemically etched, resulting in the selective removal of the latent ion tracks. Polymers such as polycarbonate (PC), polyethylene terephthalate (PET), polyimide (PI) are ideally suited for this purpose due to their high susceptibility for selective ion track-etching and their good mechanical and chemical strength for practical applications. It is clear that transparency of the porous membrane will depend on various factors such as the base material, the pore size, the pore density and the angle of irradiation. Furthermore, the pore size (10 nm to 30 µm), density (1×10^3 pores cm^{-2} to 1×10^{10} pores cm^{-2}), orientation and shape can be varied in a controllable manner.

In the frame of HEPSTEM, track-etched hydrophilic polycarbonate membranes were purchased from it4ip. The membranes are manufactured from high-quality polycarbonate films with a smooth surface, have a narrow pore size distribution and well-controlled pore shape. To allow for maximum transparency, the pores



(a) (b)

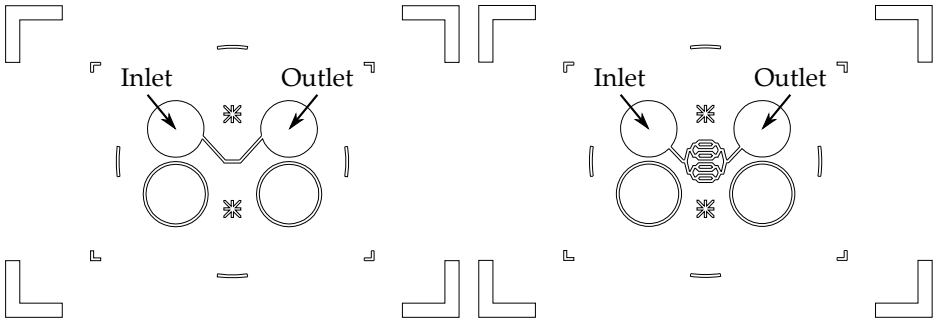
Figure 6.18: Surface topography of the selected polycarbonate membranes.

are oriented perpendicular to the membrane surface. Membrane thickness can vary over a wide range from 5 µm up to 100 µm; membranes with thicknesses of 7 µm and 24 µm were selected. Taking into account the size of the targeted cells, i.e. hepatic sinusoidal endothelial cells and hepatocytes, and a margin which covers the ability of the cells to deform, cylindrical pores with diameters smaller than 3 µm were considered. Initial pore density was selected to be 2×10^6 pores cm^{-2}. The surface topography of the selected polycarbonate membranes is shown in Figure 6.18.

Design and fabrication

The bioreactor is designed and fabricated in multiple stages, gradually increasing complexity by introducing an increasing number of PDMS microfluidic layers. Both single-channel and multi-channel bioreactor designs are used, as displayed in Figure 6.19. The channel heights are fixed at 100 µm, while channel widths of 50 µm and 100 µm are included.

Single-layered bioreactor The first version of the bioreactor consisted of a single microfluidic layer bonded to a glass microscope slide; no porous membranes are used. The purpose of this bioreactor is to evaluate and fine-tune the design, but also to develop the protocols for cell seeding and cell culturing.
The fabrication is started by mixing Silastic® MDX4-4210 base and curing agent in a 10:1 ratio by weight, respectively. Well-mixed, degassed liquid PDMS prepolymer is subsequently poured on the SU-8 master mold, degassed and cured for 48 h at room temperature. The cured PDMS slab is then peeled from the SU-8 master mold (Figure 6.20) and cut with scissors along the design outline, indi-

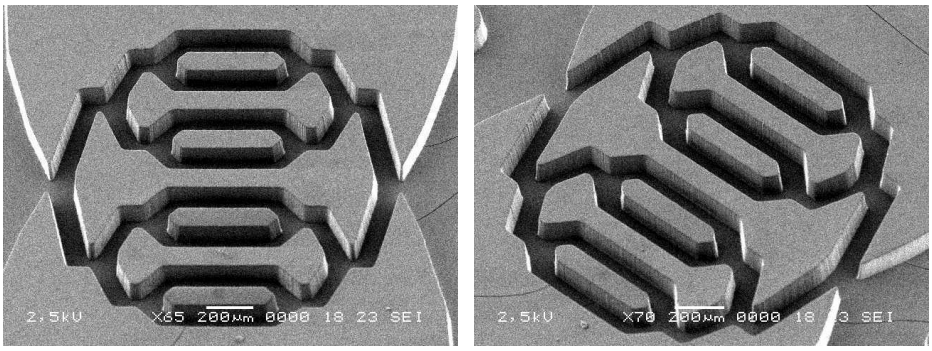


(a) Single-channel design. (b) Multi-channel design.

Figure 6.19: Single-channel and multi-channel bioreactor designs.

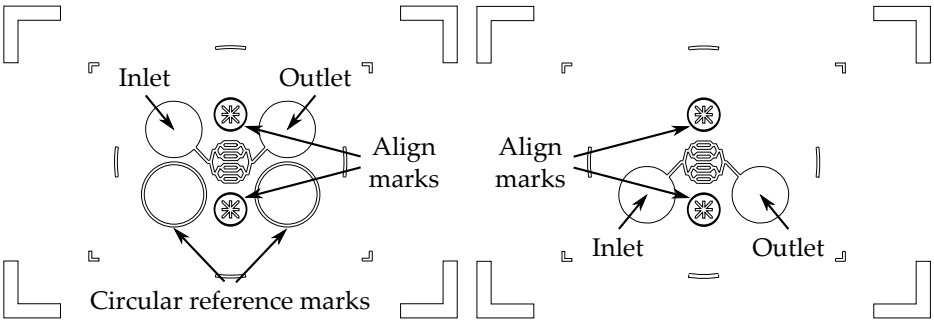
cated by the 'L'-shapes in Figure 6.19. Holes are punched through the channel inlet and outlet of the microfluidic layer using a 2 mm diameter biopsy punch (Dermat Medical Supplies NV). The microfluidic layer is then exposed to an oxygen plasma and bonded to a glass microscope slide. Finally, extruded FEP tubing (Zeus; Table 5.4) is applied using the procedure described in Section 5.2.5.

Two-layered bioreactor Two-layered bioreactors are composed of two PDMS microfluidic layers which are aligned relative to each other and bonded to the porous membrane. The purpose of this bioreactor is to allow culturing of two juxtaposed cell types. Examples for the top layer and bottom layer design are illustrated in Figure 6.21.
Both microfluidic layers, i.e. the top and bottom PDMS microfluidic layers, are fabricated using an identical procedure as the one described for the single-layered bioreactor. Holes are punched solely through the top microfluidic layer at the location of the channel inlet and outlet, but also through the circular reference marks which indicate the position of the inlet and outlet of the bottom microfluidic layer, using a 2 mm diameter biopsy punch (Dermat Medical Supplies NV).
After coating the porous membrane with a 50 nm thick layer of SiO_2 (Section 5.3.2), the top microfluidic layer and SiO_2 coated porous membrane are exposed to an oxygen plasma and bonded. This is illustrated in Figure 6.22; it is also noticed that the pores run through the membrane cross section, perpendicularly to the membrane surface. Holes are then punched through the porous membrane to provide direct access to the inlet and outlet of the bottom microfluidic layer. Next, the bottom microfluidic layer and the second side of the porous membrane are exposed to an oxygen plasma, aligned and bonded. This is illustrated in Figure 6.23. Finally, extruded FEP tubing (Zeus; Table 5.4) is applied using the procedure described in Section 5.2.5.



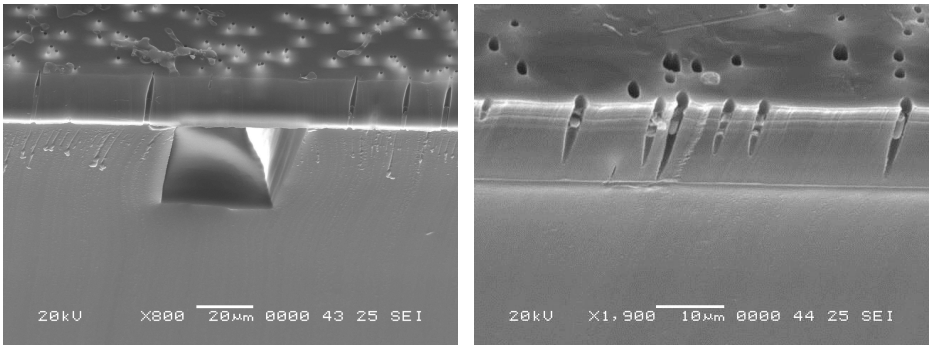
(a) (b)

Figure 6.20: Multi-channel design transferred to Silastic® MDX4-4210; 100 µm high channels.



(a) Top layer design. (b) Bottom layer design.

Figure 6.21: Two-layered bioreactors are composed of two PDMS microfluidic layers which are aligned relative to each other.



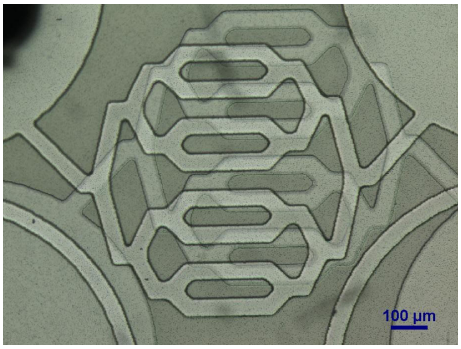
(a) (b)

Figure 6.22: Cross section of a microfluidic layer bonded to an SiO_2 coated porous polycarbonate membrane.

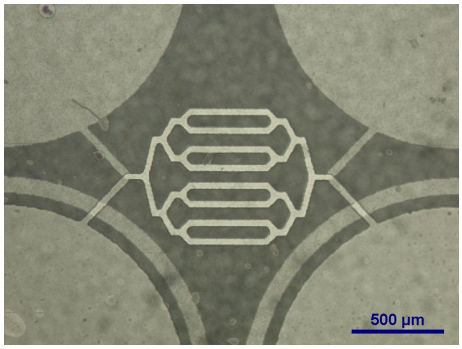
Multi-layered bioreactor The bioreactors composed of more than two microfluidic layers require the fabrication of so-called perforated PDMS microfluidic layers, i.e. micropatterned PDMS layers without capping, as depicted in the center of the schematic cross section shown in Figure 6.15. The fabrication of such perforated PDMS microfluidic layers is being developed and optimized within the PhD of Amir Jahanshahi.

Operation

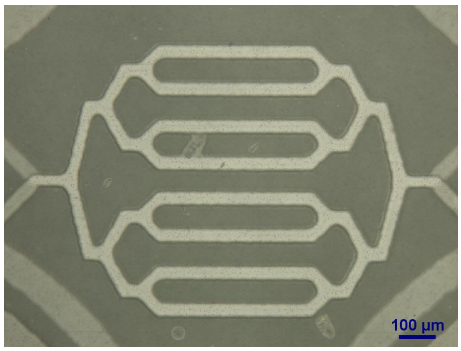
The flow of liquids in the microfluidic devices can be controlled using several external systems, such as peristaltic pumps, syringe pumps or pressure generators. These external systems are connected to the microfluidic device via the FEP tubing. Due to the small volumes inside the microfluidic channels, very small flow rates are desired. Consider, for example, a channel with cross-sectional dimensions of 100 µm by 100 µm, and a channel length of 10 mm. The volume inside this channel is easily calculated to be as small as 100 nl. High precision syringe pumps are the most prevalent pump technology for microfluidics. Most syringe pumps are able to offer a uniform flow with limited pulsation, and are capable of achieving picoliter per minute flow rates, ideally suited for microfluidic devices considering the small liquid volumes.
The setup available at the CMST research group is displayed in Figure 6.24. A syringe with luer lock tip is mounted in a HP-540060 infusion / withdrawal syringe pump (TSE Systems GmbH); the detailed specifications of the latter can be reviewed in the product data sheet [12]. The minimum and maximum achievable flow rate are 0.001 µl h^{-1} with a 1 µl syringe and 2120 ml h^{-1} with a 60 ml syringe,



(a) Not aligned.

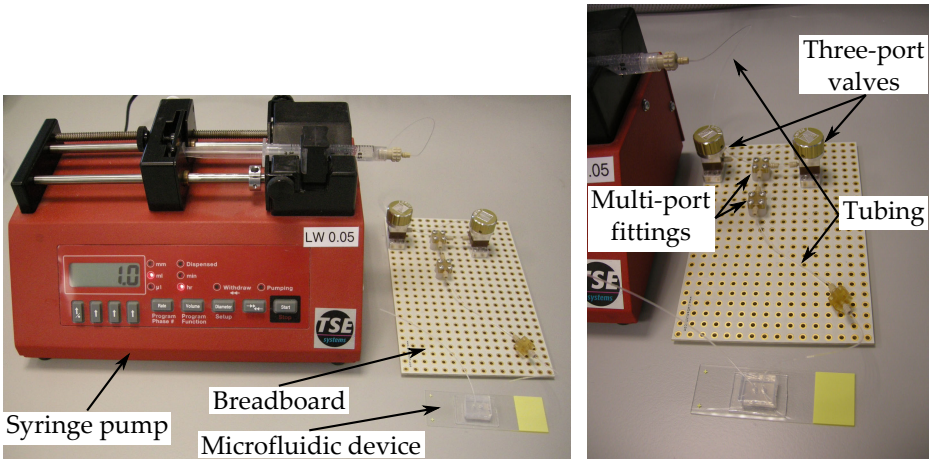


(b) Aligned.



(c) Aligned.

Figure 6.23: Aligning and bonding of two microfluidic layers, separated by a porous membrane.



(a) Setup for microfluidics.

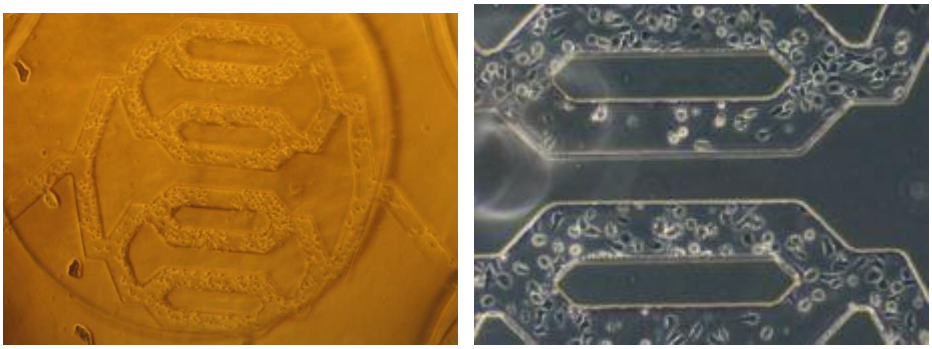
(b) Breadboard with fluidic components.

Figure 6.24: The setup for microfluidics available at CMST.

respectively. The syringe is connected to the FEP tubing via a luer lock adapter and a so-called one-piece fitting (LabSmith, Inc.) which is suited for connecting tubing with an outer diameter of 1/32 inch. External fluid control is enabled by introducing a breadboard (LabSmith, Inc.) in between the syringe and the microfluidic device. Several fluidic components, such as three-port valves and multiport fittings, are mounted on the breadboard (Figure 6.24(b)).

Cell seeding

At the time of writing of this dissertation, single-layered microfluidic bioreactors were being tested for cell culture compatibility both at the Stem Cell Institute Leuven (SCIL) of the KU Leuven (KUL), and the Liver Cell Biology Lab (LIVR) of the Vrije Universiteit Brussel (VUB). To perform cell seeding and medium perfusion, an identical setup was used as described in previous section. This setup offers the possibility to place the microfluidic bioreactor and the breadboard in an incubator, and to easily move them around as required e.g. for optical microscopy. Although the exact procedure and evaluation of the cell seeding falls beyond the scope of this PhD dissertation, Figure 6.25 illustrates the successful seeding of human embryonic stem cells in the microfluidic bioreactors, performed at the Stem Cell Institute Leuven.



(a) First day after cell seeding. (b) 3 h after cell seeding.

Figure 6.25: Human embryonic stem cells seeded in single-layered microfluidic bioreactors (performed at Stem Cell Institute Leuven of the KU Leuven).

6.4 Conclusions

A number of applications enabled by and benefiting from the technologies which were presented in the previous chapters have been highlighted. Both elastic microsystems with modular functionalities and PDMS-based microfluidics for cell culturing have been discussed.
Elastic microsystems with modular functionalities have been discussed within the frame of the IWT-SBO funded project BrainSTAR. The applicability of the technologies presented in Chapter 3 and Chapter 4 was illustrated by designing and fabricating a technology demonstrator using a commercially available MSP430F1611 microcontroller chip from Texas Instruments. The full functionality of the different components was demonstrated.
PDMS-based microfluidics for cell culturing has been discussed within the frame of the IWT-SBO funded project HEPSTEM. A so-called micro-hepatic sinusoid bioreactor was developed which has a cellular architecture closely resembling that of the liver *in vivo*. Specific attention was spent to the integration of porous membranes in a microfluidic environment, using the techniques presented in Chapter 5. The successful seeding of human embryonic stem cells in preliminary bioreactors was demonstrated.

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7 Conclusions and final remarks

7.1 Conclusions

Recent developments in the field of electronics packaging have resulted in the use of materials and technologies which enable the design and fabrication of mechanically deformable electronic systems, allowing e.g. the shaping to a desired three-dimensional shape. The work presented in this dissertation focused on the development of a technology platform for the realization of conformable, stretchable thin electronic systems, embedded in a thin biocompatible silicone elastomer. As this material is also frequently used for the fabrication of microfluidic systems, the presented platform can thus be used to develop solutions for the requirements of diverse biomedical applications. The use of thin-film microfabrication techniques allows characteristic dimensions down to the order of tens of micrometers, which is sufficient for even the most demanding applications.

The development of the conformable, stretchable electronics platform was tackled in two phases. In a first phase, a fabrication process for stretchable electrical interconnections was established. Next, in a second phase, the interconnections were combined with thinned dies. Thin-film gold metallization was chosen as conductor, as this enables biomedical applications. Furthermore, it allows for fine interconnection pitches and feature sizes, making it directly compatible with the bond pad pitches of conventional, commercially available dies.

Stretchable electrical interconnections were achieved by patterning the gold metallization into a sequence of horseshoe shapes, which are able to function as 'two-dimensional springs' when embedded in a silicone elastomer. Polyimide

was introduced around the meandering conductors, and follows the meandering configuration; it serves as a support for the stretchable interconnections. Using dedicated test structures, these were shown to exhibit excellent mechanical performance. Reversible stretching of the interconnections at uniaxial strains up to 100 % was illustrated. Cyclic mechanical loading clearly highlighted the impact of the polyimide support width on the reliability: by increasing the polyimide width relative to the conductor width, the lifetime of the interconnections is increased greatly. This was clearly illustrated at large strains of 60 %, 40 % and 20 %. At strains of 10 %, the interconnections were shown to have a minimum lifetime of 500 000 cycles.

Functional ICs were combined with the stretchable electrical interconnections by thinning the unpackaged dies from their original thickness to thicknesses as small as 20 µm - 30 µm, and embedding them in between several spin-on polyimide films. By encapsulation in a silicone elastomer, a system is achieved that can stretch and flex, the latter even at the location of the non-stretchable islands. The presented methodology avoids the use of conventional bulky packaged dies (e.g. SMD), and improves the miniaturization and the conformability of the electronic system. The process was designed to enable simultaneous fabrication of the stretchable electrical interconnections and packaging of the thinned dies. All processing steps are compatible with thin-film processing.

The process yield was characterized using electrical conductivity measurements performed on daisy chain silicon dies. The reliable character of the technology was pointed out by a via yield of 99.82 %. It was also demonstrated that the daisy chain dies can be replaced by commercially available unpackaged chips, such as the MSP430 microcontroller chips from Texas Instruments. A technology demonstrator was designed and fabricated using this microcontroller. Both the ability to program the microcontroller after embedding, and the full functionality were demonstrated. The developed platform thus enables the fabrication of conformable, stretchable electronic circuits for the most diverse applications.

Both fabrication processes were developed so that the encapsulation in the silicone elastomer is performed at a final stage. This approach offers the advantage that diverse types of silicone elastomers (e.g. biomedical grade) or even other elastomers (e.g. polyurethanes) can be used. A customized release technique was developed which is compatible with the typical high-temperature curing profiles of polyimides in order to successfully apply this approach.

Technologies both for single- and multi-layer PDMS-based microfluidics were developed. A combination of soft-lithographic techniques for the micropatterning and plasma treatments for the surface modification of PDMS were used to create microfluidic channels. The master molds were fabricated via SU-8 photolithography, allowing for a wide range of feature sizes down to the order of single cell sizes. Furthermore, a custom developed aligning technique for multiple microfluidic layers successfully minimized the aligning error caused by shrinkage of PDMS during curing.

The specific interest of microfluidics for cell culturing was illustrated in the context of liver-related research. Micro-hepatic sinusoid bioreactors were fabricated, with cellular architectures closely resembling that of the liver *in vivo*. To this end, a methodology was developed using thin SiO2 coatings, allowing the heterogeneous integration of various membranes in the microfluidic environments. The successful seeding of human embryonic stem cells in the micro-hepatic sinusoid bioreactors was demonstrated.
The dual integration of microfluidics and microelectronics was demonstrated. A technology demonstrator was fabricated comprising a light source and detector integrated on both sides of a microfluidic channel. The packaging of the light source and detector array chips, and the fabrication of the microfluidic channels was performed separately without influencing each other. Both were combined only in the final stage.
In conclusion, a generic technology platform has been developed for the integration of microelectronics and microfluidics on stretchable substrates. Specific attention was spent to obtain a modular approach: the multiple functional building blocks are fabricated separately without influencing each other, and can be combined only in the final stage.
A concise overview of the realizations in this research can also be found in Table 7.1. It highlights the achievements with respect to the initial goals set out in the scope and goals (Section 1.3).

7.2 Outlook and recommendations for future work

The generic technology platform presented in this dissertation was not developed in the frame of a well-defined target application. This was certainly beneficial for the generic character. Diverse technology demonstrators were realized, though it is expected that working towards a well-defined target application would fully demonstrate the capabilities of the presented technologies.
Taking into account the large amount of biomedical applications which clearly benefit, an elaborate biocompatibility study imposes itself. In this context, the use of other metals such as platinum might be considered, as these are generally considered to be more biocompatible.
The realized stretchable electrical interconnections were shown to exhibit great mechanical performance. It is, however, expected that the mechanical performance can be even further improved by gaining insight into the failure mechanisms of the interconnections. Also the use of parallel, fine-line bridged horseshoe shaped interconnections (Section 2.2.2) is an interesting topic for future research.
As might be required by certain applications, measures might have to be investigated to lower the relatively high electrical resistance inherent to the stretchable thin-film gold conductors. This can be achieved by increasing the thickness of the

Goals	Achievements
Stretchable interconnections which are able to accommodate strains of 20 %	Meandering horseshoe shaped metallic conductors have been realized which can be reversibly stretched up to two times their original length
Reversibly stretchable interconnections with lifetimes in the order of 10^5 to 10^6 straining cycles at strains of 10 % to 20 %	Minimum lifetimes of 130 000 cycles and 500 000 cycles at strains of 20 % and 10 %, respectively, have been demonstrated
Combination of the stretchable interconnections with unpackaged, thinned dies	A methodology is described in Chapter 4 and demonstrated with an MSP430 microcontroller from Texas Instruments
Minimum achievable metallization pitches in the order of 50 µm	Metallization pitches down to 45 µm have been illustrated using the test design displayed in Figure 3.11
Integration of porous membranes in PDMS-based microfluidics	A methodology using SiO_2 coatings has been developed to integrate track-etched polycarbonate membranes
Integration of microelectronics in PDMS-based microfluidics	A technology demonstrator composed of a light source and detector integrated on both sides of a microfluidic channel has been realized
Modular approach, both for the stretchable electronics and the microfluidics	The platform allows for combination of the individual, independently realized building blocks
Avoiding cytotoxic materials	The used materials are non-cytotoxic
Evaluation of all individual modules	All individual modules have been evaluated at intermediate stages
Compatibility of all processing steps with conventional equipment for microelectronics processing	Conventional equipment for microelectronics processing has been used throughout the processes

Table 7.1: Comparison of the initial goals and achievements.

gold conductor, e.g. via electroplating. This requires the fabrication processes to be adapted accordingly, while the mechanical and electrical performance needs to be re-evaluated.
The developments for the conformable, stretchable electronics platform concentrated on the packaging of a single thinned chip. Practical applications, however, commonly require the integration of various chips. Several routes can be considered to achieve this; multiple thinned chips can be embedded simultaneously, or they can be combined after packaging the single chips. In this context, double-layer metallization (whether or not stretchable) is of interest for obvious reasons of routing.
Microfluidic platforms have been receiving more and more attention in the field of biology. This is also noticed within the CMST research group; several ideas have originated from discussions with different research groups. Working towards the diverse applications will certainly require fine-tuning of the current available technologies, or require the adding of different components such as mixers, valves or pneumatically actuated membranes.
Working towards industrialization still requires multiple points of attention. During the development of the processes, care is taken to keep all processing steps compatible with conventional equipment for microelectronics processing. However, it has to be noted that polyimide is a rather expensive polymer. Therefore, cheaper alternatives for the polyimide might be desired. In addition, commercially available products will have to meet specific requirements concerning e.g. the reliability or the biocompatibility, which are highly dependent on the application the product is developed for. It is clear that such requirements are thus ideally tested by mimicking the corresponding environment.